

CMOS Latchup Simulation



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Introduction

- Triggering of parasitic pnpn structure across CMOS well boundary
- Evaluation of different well dopings and depths
- Evaluation of different epi thicknesses
- Optimize p+/n+ spacing



Process Simulation Requirements

- Accurate process and device simulation of large structures
- Easy way to adjust p+/n+ spacing
- Consistent mesh with different p+/n+ spacing
- Interface whole structure to device simulator



Device Simulation Requirements

- Ability to handle large structures
- Ability to trigger latchup in DC and transient mode
- Tracing of complex I-V curves
- Appropriate physical models for pnpn devices

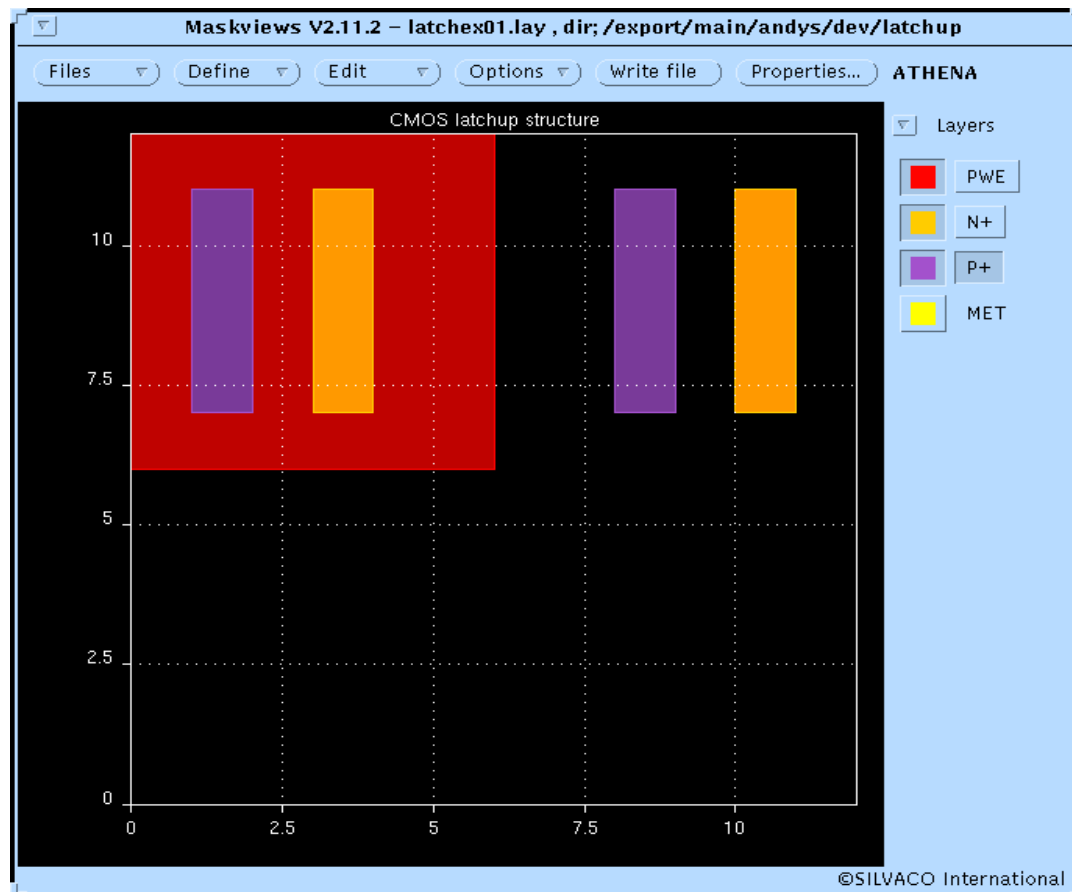


Case Study

- Use MaskViews layout interface to construct a pn well boundary with mesh spacing tied to mask edge locations
- Use ATHENA process simulation to simulate structure
- ATLAS simulation of latchup by:
 - positive DC ramp on Vdd
 - negative DC ramp on Vss
 - transient pulse on Vss
- Post processing analysis

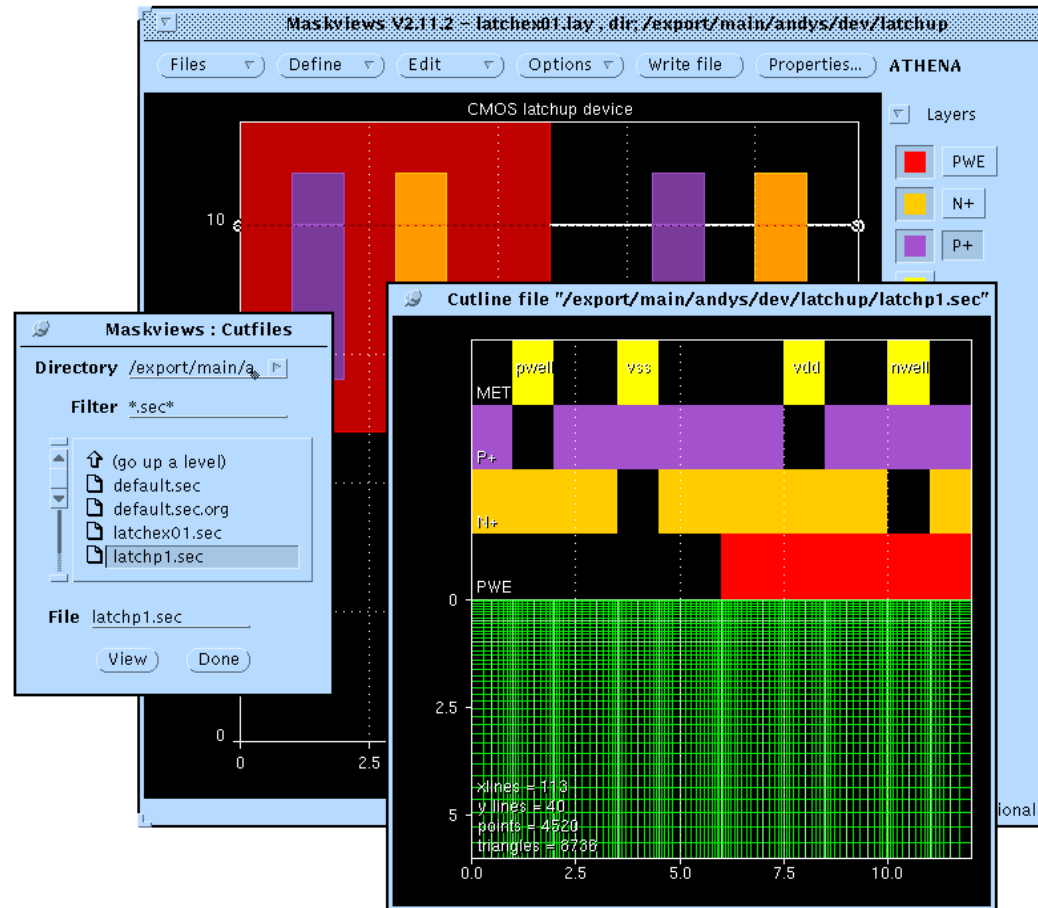


Layout of P+/N+ Well Boundary



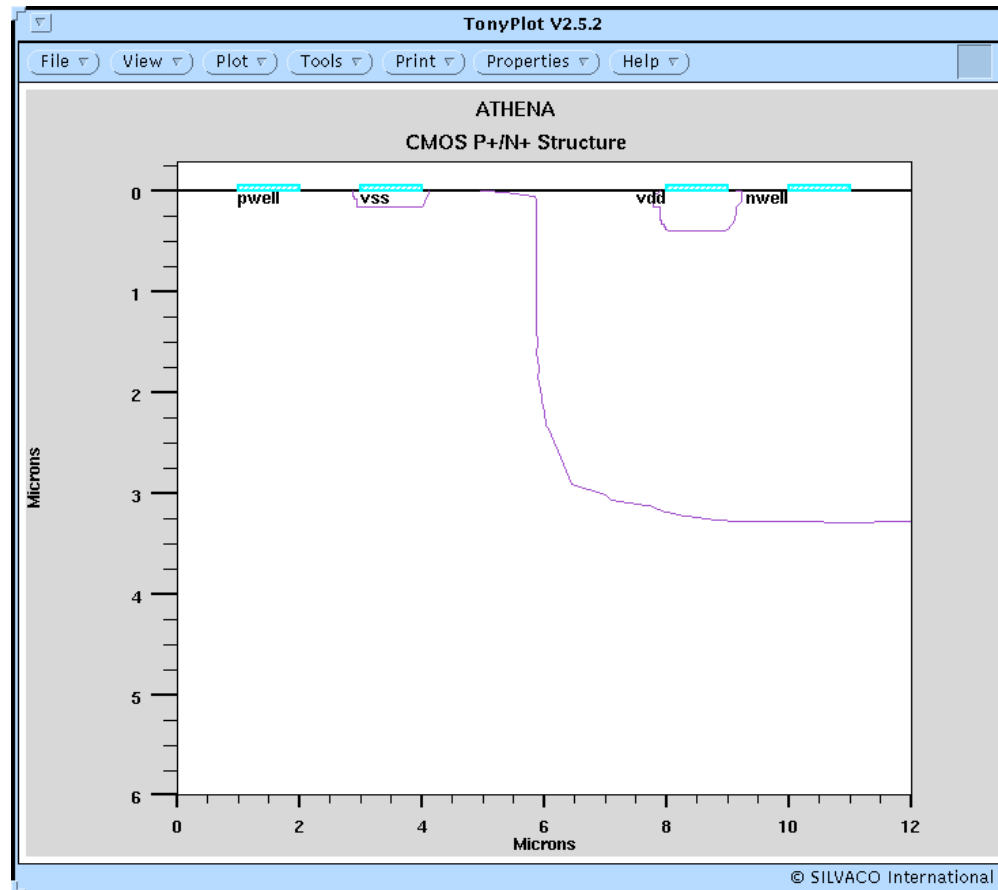


Mask Edges and Grid for 2D Cross Section of Layout



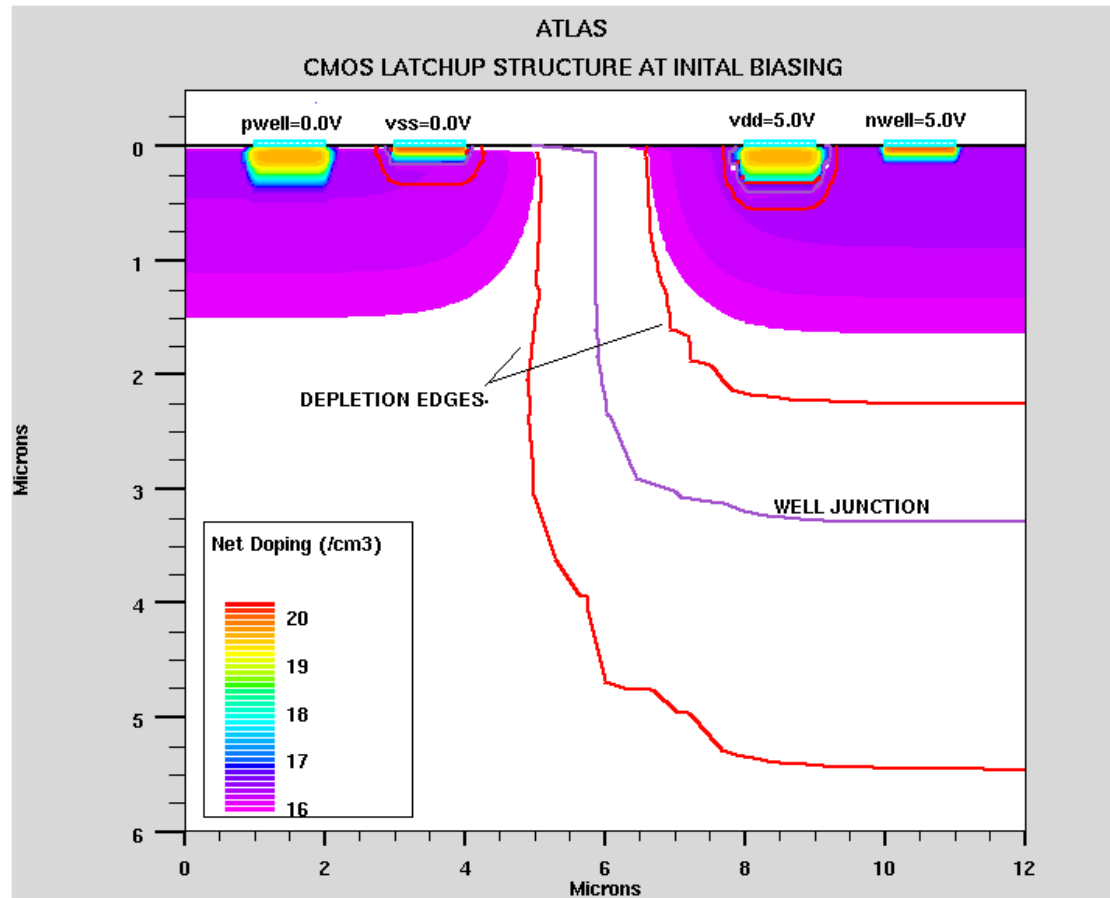


Final Process Structure with Junctions





Final Process Structure with Doping and Depletion Regions





Device Simulation Model Requirements

- CMOS latchup is a bipolar phenomena
- Requires bipolar model set including accurate recombination models
- Requires band gap narrowing for accurate prediction of parasitic device gain

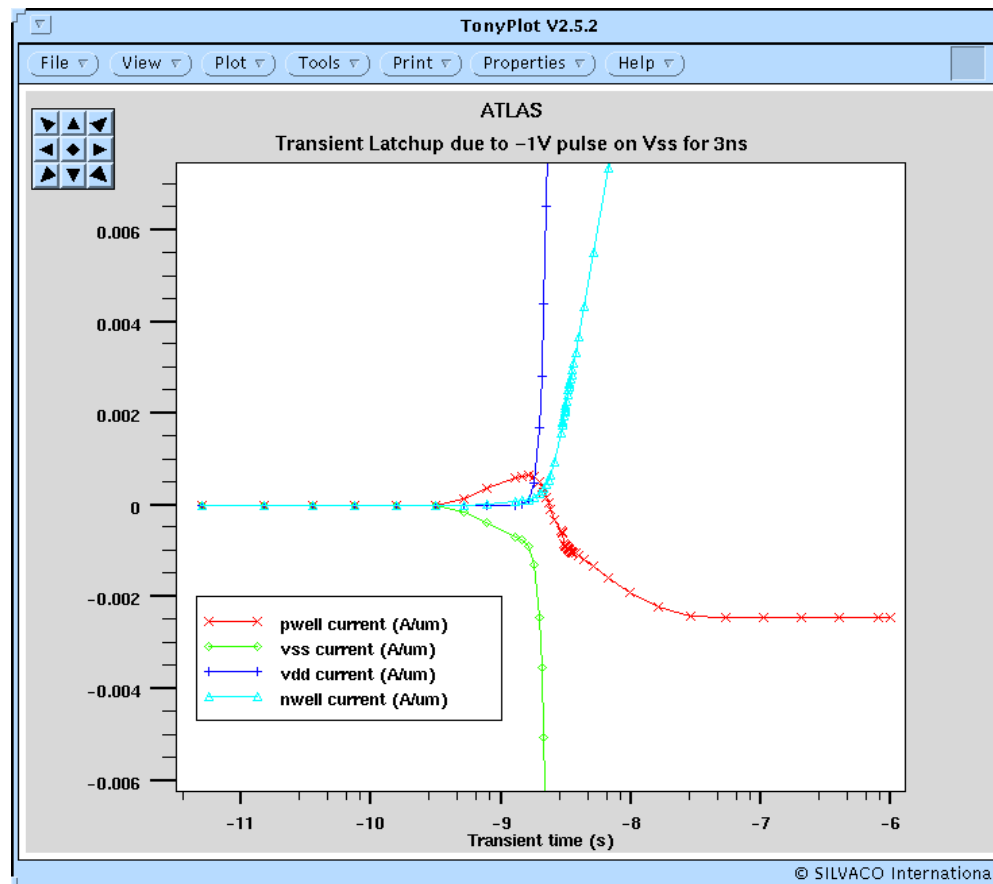


Transient Device Simulation Setup

- 1/ bias Vdd and Nwell to 5V
- 2/ apply -1V pulse to Vss for several nanoseconds
- 3/ return Vss to zero continue simulation for 1us
- 4/ Analyze current-time plot to analyze trigger point

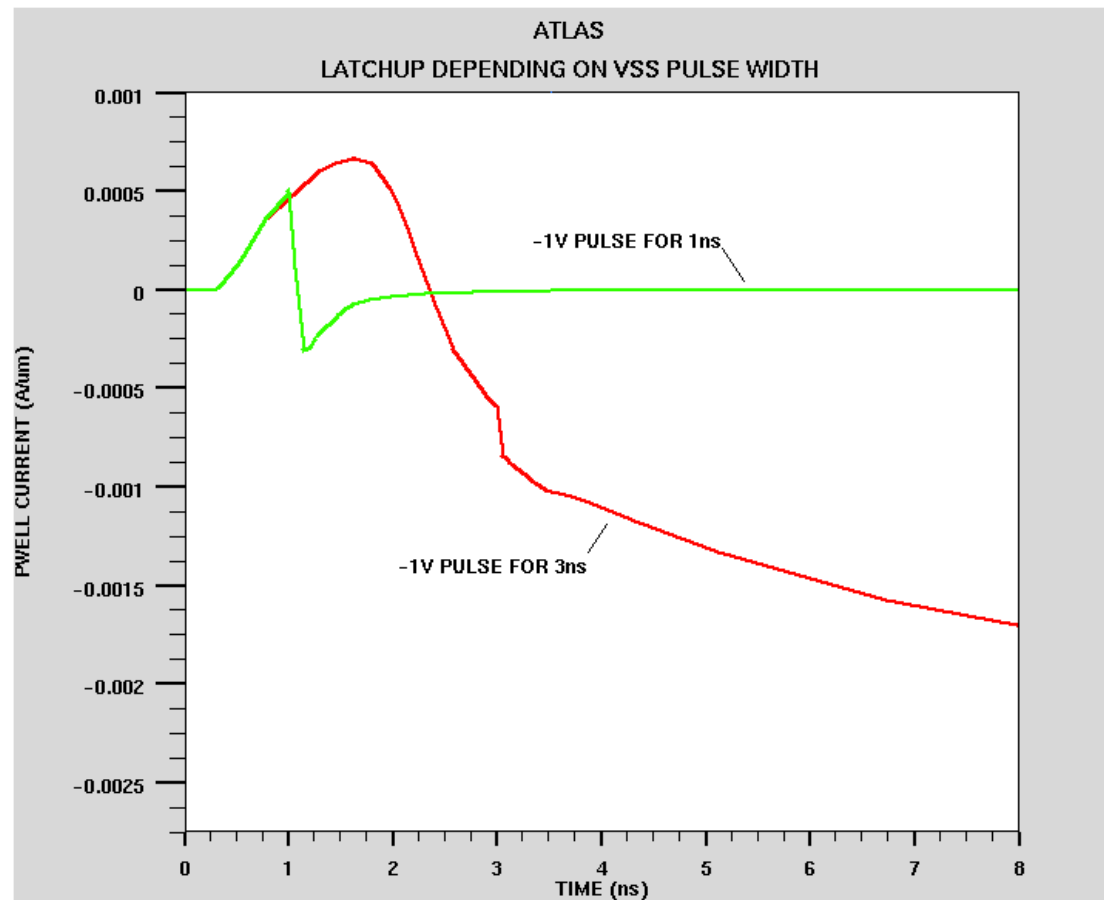


Current vs. Time During Transient latchup



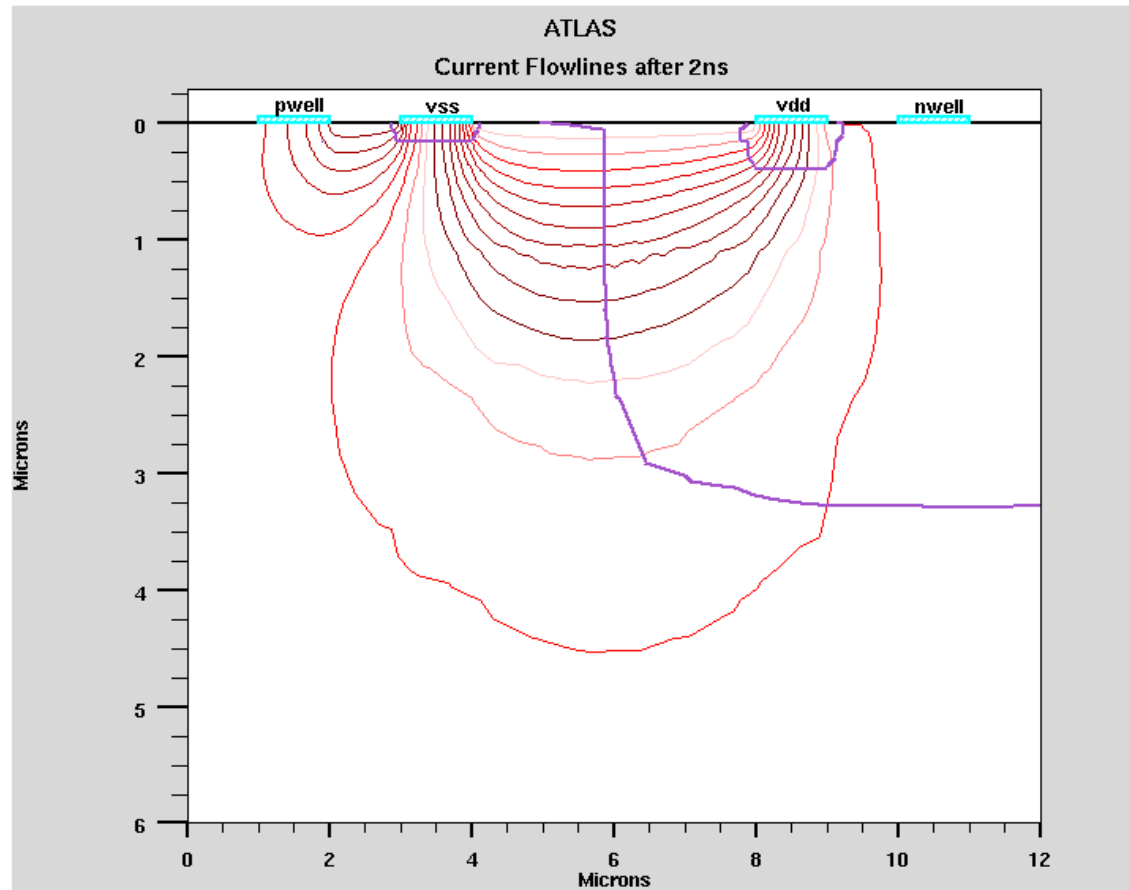


Comparison of 1ns and 3ns Duration Pulses



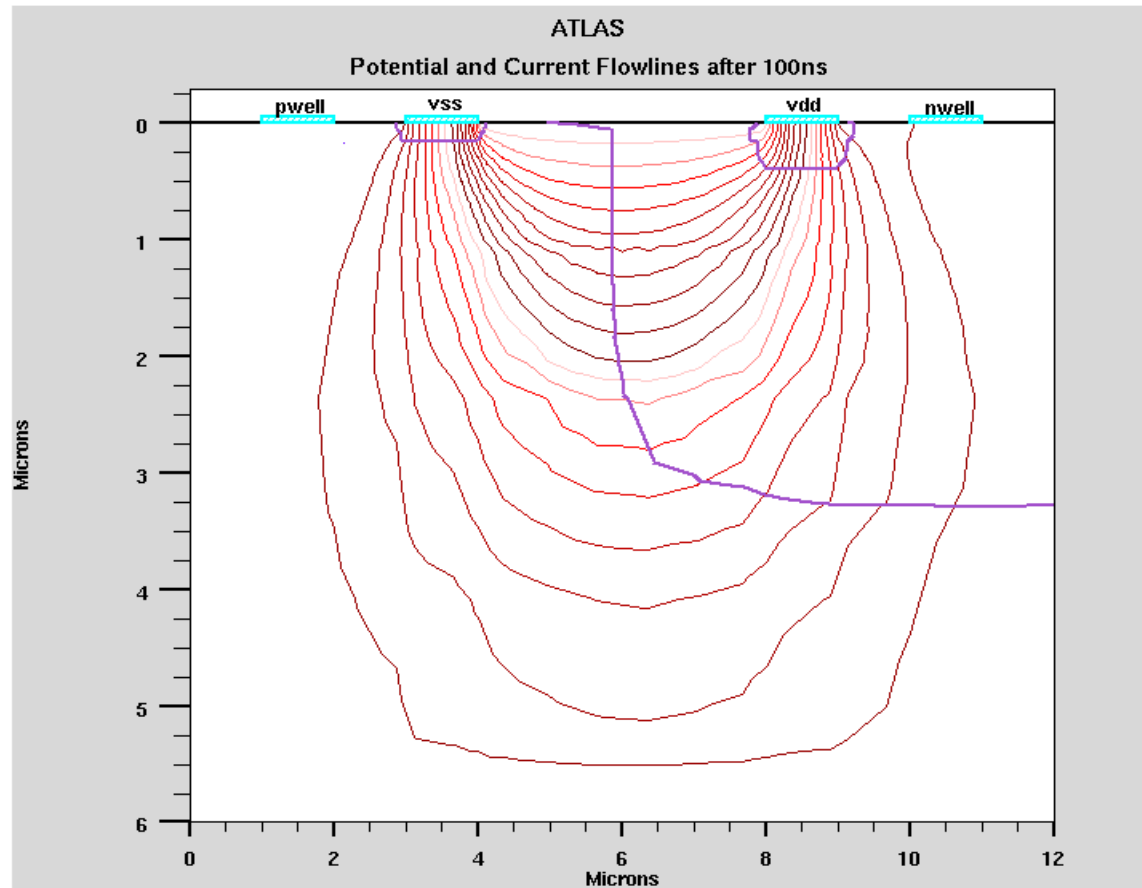


Flowlines in Structure During Vss Pulse





Flowlines in Latched Structure



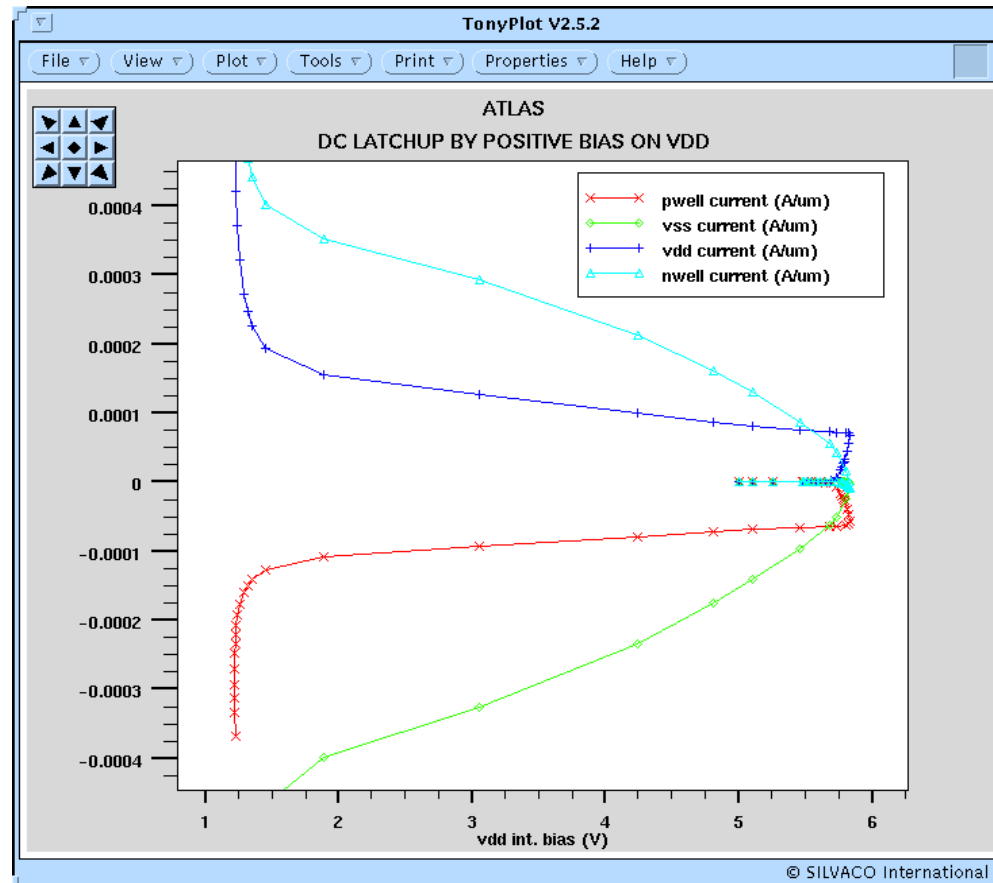


DC Latchup Simulation Setup

- 1/ bias Vdd and Nwell to 5V
- 2a/ apply positive bias ramp to Vdd, trace curve until $I_{dd}=1\text{mA}/\mu\text{m}$
- 2b/ apply negative bias ramp to Vss, trace curve until $I_{ss}=1\text{mA}/\mu\text{m}$
- 3/ analyze curve to measure trigger voltage and holding current

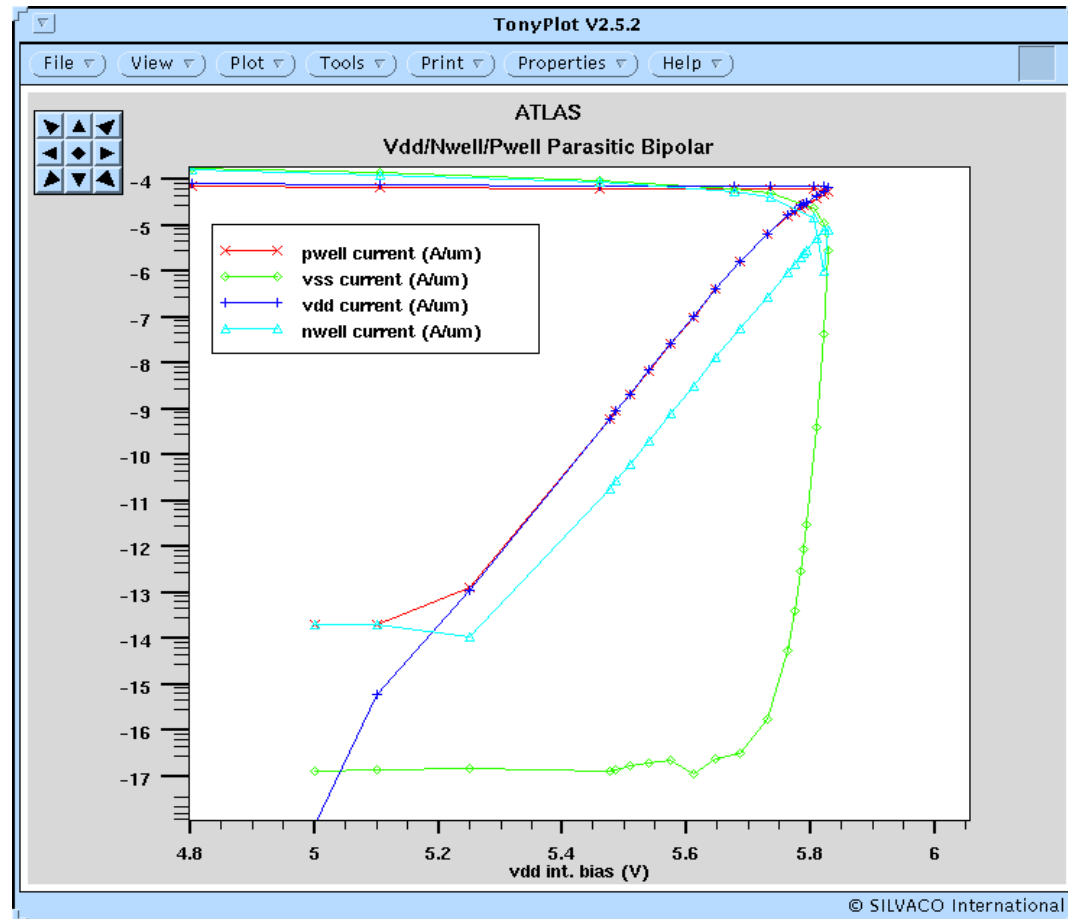


Positive DC bias on Vdd



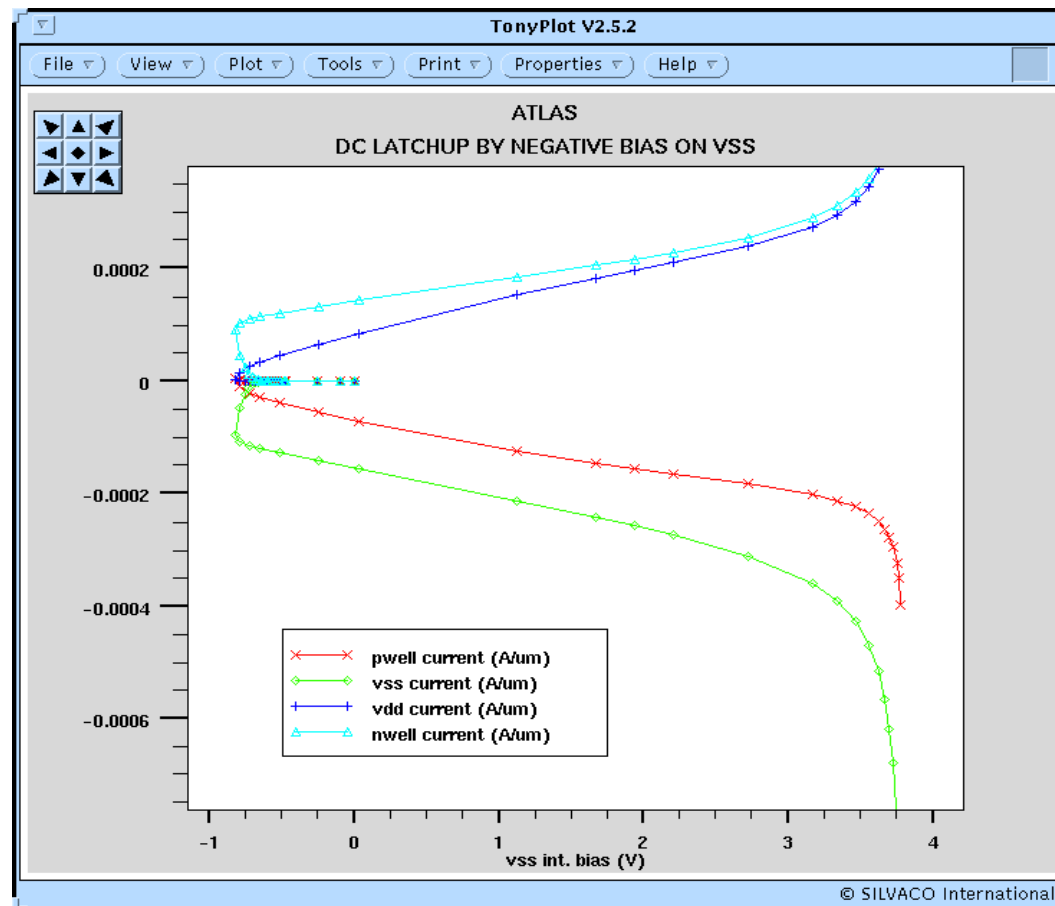


Parasitic Vertical pnp Bipolar Characteristic



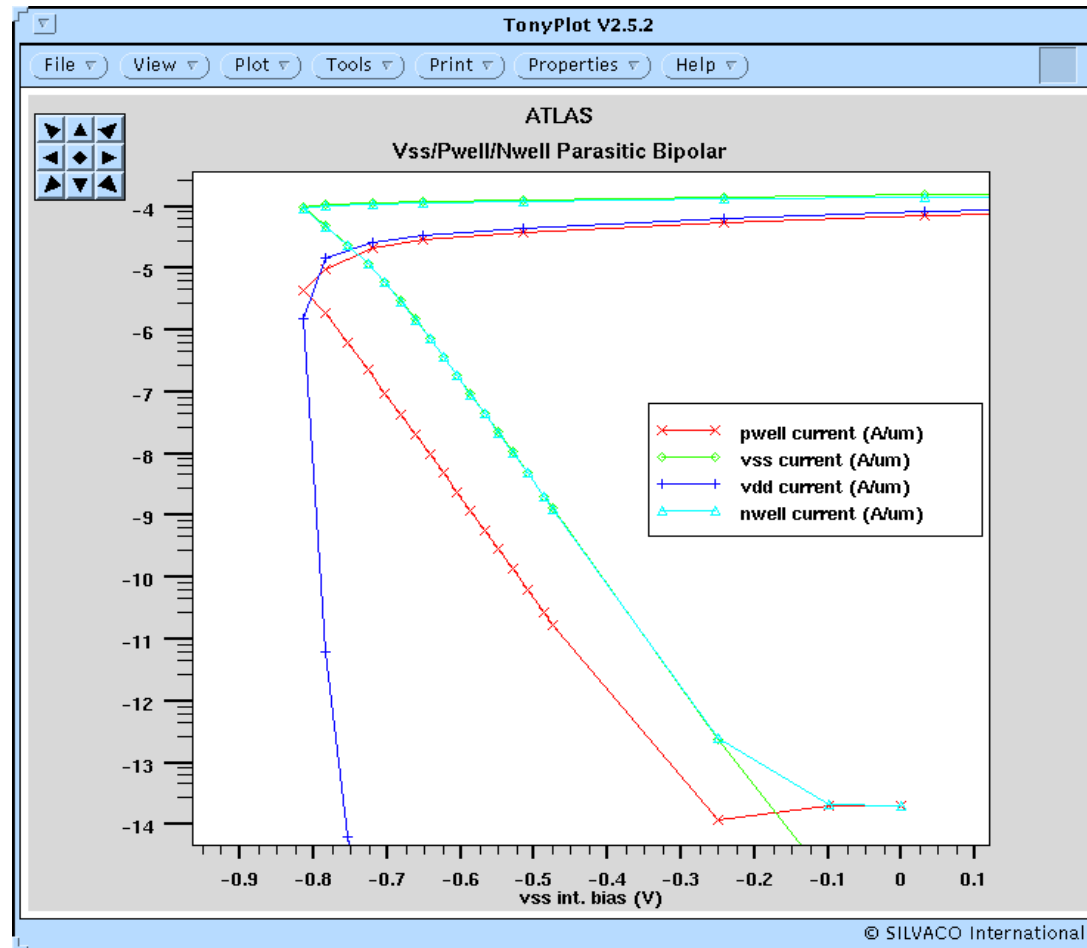


Negative DC Bias on Vss





Parasitic Lateral npn Bipolar Characteristic



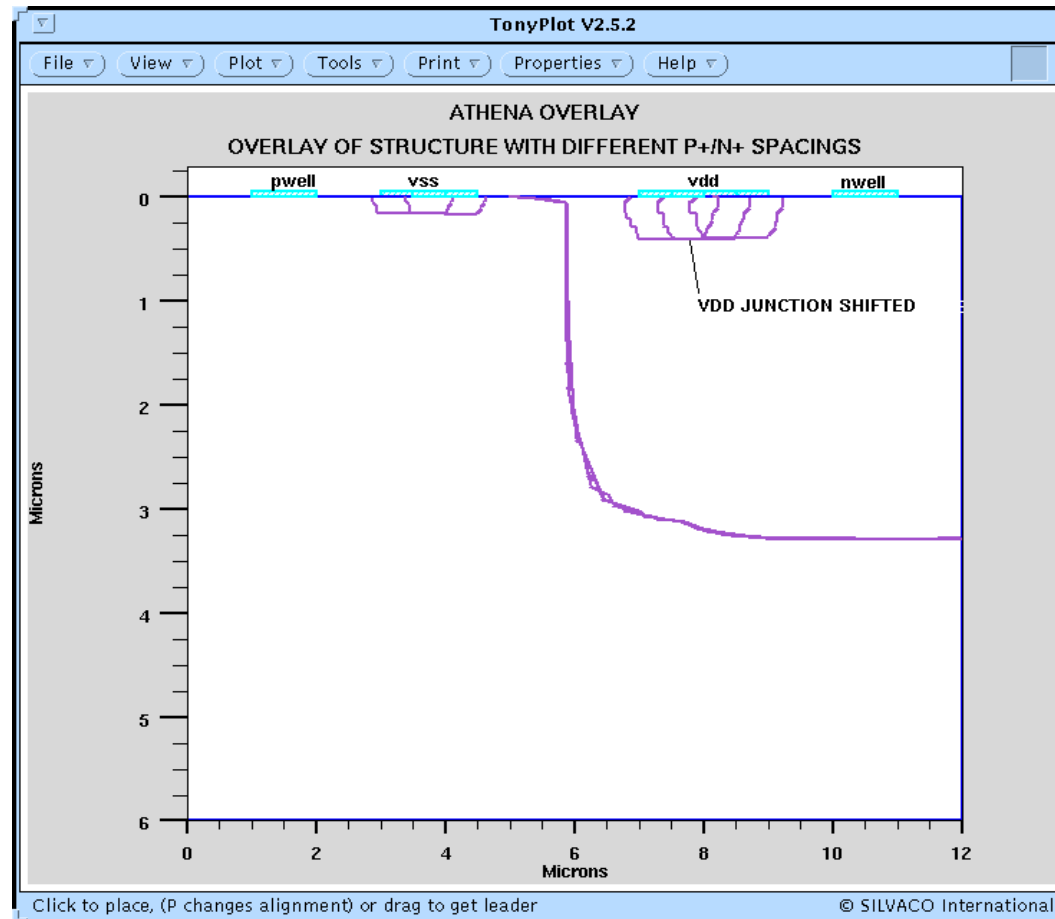


P+/N+ Spacing

- To evaluate the effect of p+/n+ spacing the simulations need to be repeated with different structures
- Changes to the p+/n+ spacing can be done in MaskViews. A new cutline for each spacing is required.
- Mesh spacing follows mask edges to ensure consistent simulation grid
- No changes to ATHENA or ATLAS input files required

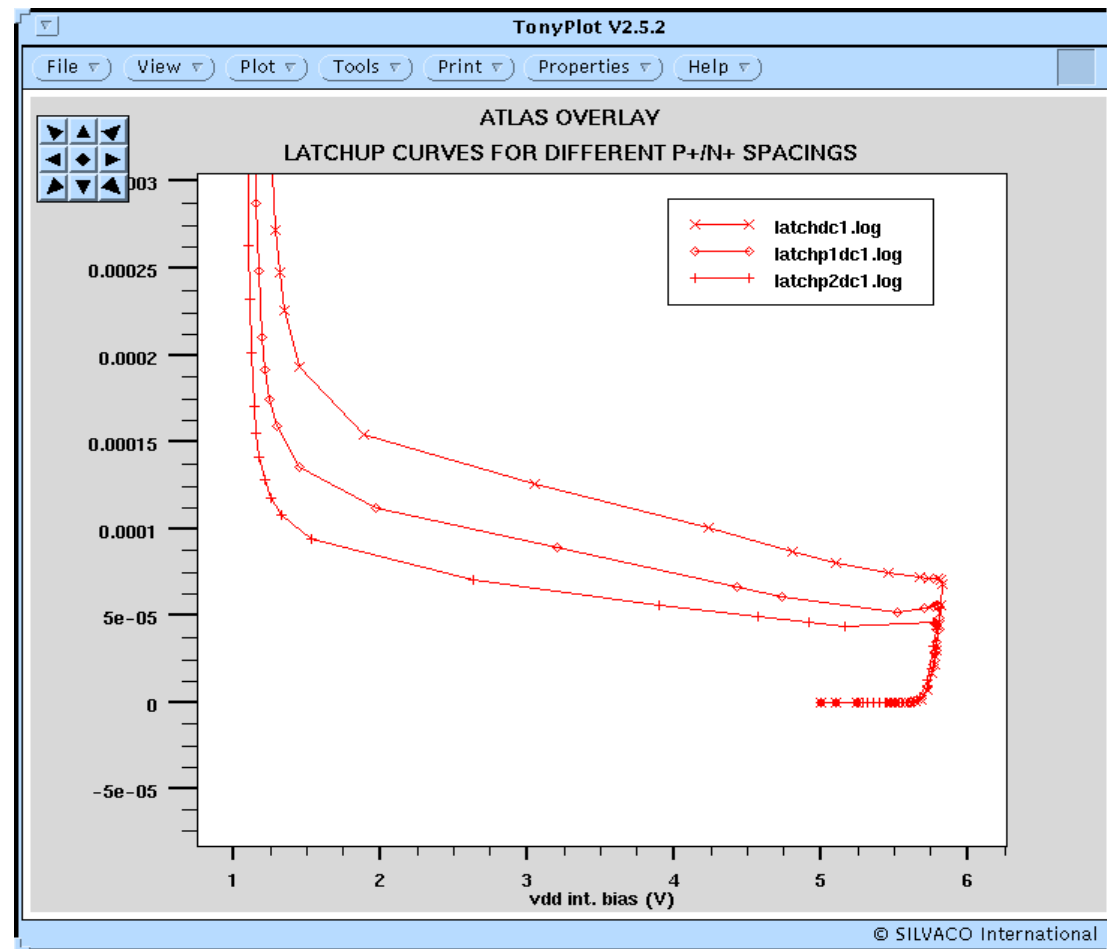


Overlay of two Structures with Different p+/n+ Spacings





Comparison of Positive DC Latchup Characteristics





Conclusion

- ATHENA and ATLAS are able to simulate CMOS latchup
- For DC latchup the CURVETRACE feature an excellent tool for extracting complex I-V characteristics
- In transient mode ATLAS can evaluate the length of pulse required for latchup
- Different p+/n+ spacings can be evaluated by using MaskViews
- More complex p+/n+ layouts can be evaluated using ATLAS/ Device3D