

Modeling of Local Oxidation Processes



SILVACO



Introduction

- Isolation Processes in the VLSI Technology
- Main Aspects of LOCOS simulation
- ATHENA Oxidation Models
- Several Examples of LOCOS structures
- Calibration of LOCOS effects using VWF
- Field Oxide Thinning Effect
- Pad Oxide Punch Through Effect
- Integrated Topography and In-Wafer Simulation of Self-Aligned LOCOS/Trench technology (SALOT)



Isolation Processes in the VLSI Technology

- Separate devices in VLSI circuits should be effectively isolated from each other
- One of the main aspects of miniaturization is shrinkage of isolation areas without degradation of isolation characteristics (leakage current, parasitic threshold voltage, etc.)
- Review of various isolation technologies can be found in:

S.Wolf “Silicon Processing for the VLSI Era”, Vol.2, Chap.2.
(Lattice Press, 1990)



Isolation Processes in the VLSI Technology (con't)

- LOCOS and its numerous variations
- Non-LOCOS Isolation
 - Trench and refill
 - Selective Epitaxy Growth (SEG)
 - Silicon-On-Insulator (SOI)
- Combination methods: LOCOS with trench, SOI with LOCOS, etc.



Main aspects of LOCOS Simulation

- The oxide thickness and shape
- The bird's beak length and shape
- The redistribution of the channel-stop dopant
- Stress induced in silicon during the LOCOS process
- ATHENA successfully handles all four aspects for variety of LOCOS structures



ATHENA Oxidation Models

- Compress (stresses are not taken into account)
 - Can be used for all cases but may fail to accurately predict shape and dimensions of LOCOS
- Viscous (Stress in oxide and nitride are included)
 - Capable of predicting actual bird's beak shapes and stress induced effects
 - Needs serious parameter calibration efforts
 - Much slower than compress method

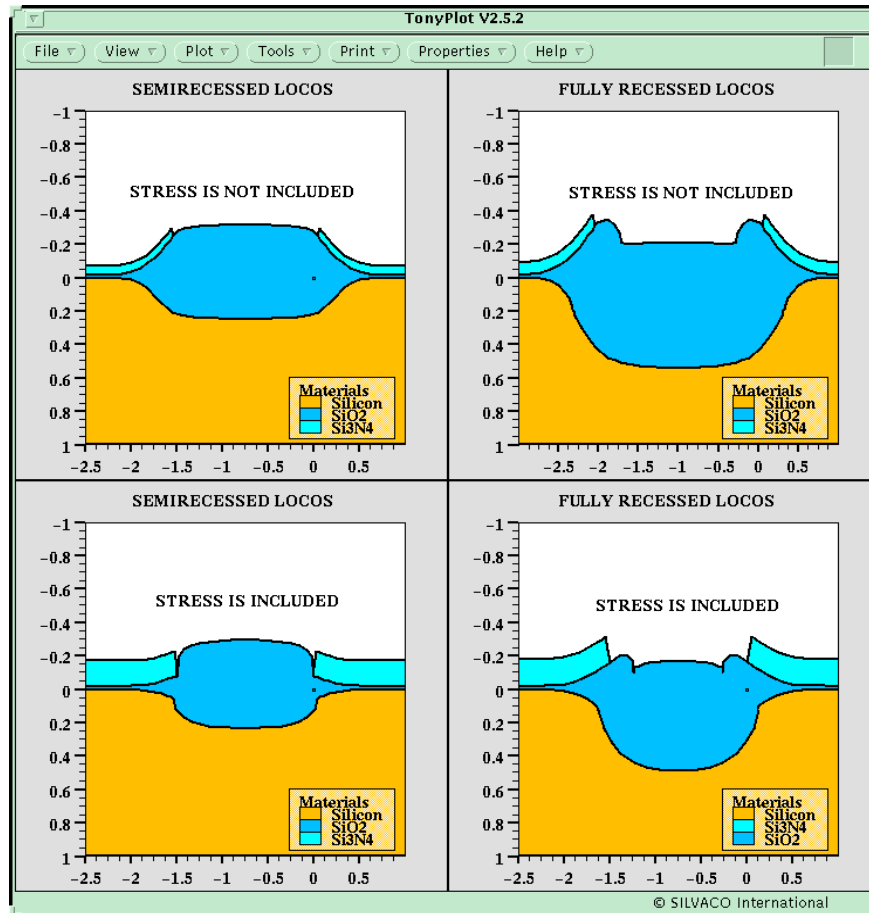


Examples of LOCOS Structures

- Semi-recessed and fully recessed LOCOS (Figure 1)
- Polybuffered LOCOS (PBL) (Figure 2 and Figure 3)
- Sealed-Interface Local Oxidation (SILO) (Figure 4)
- Sidewall-Masked Isolation (SWAMI) (Figure 5 and Figure 6)

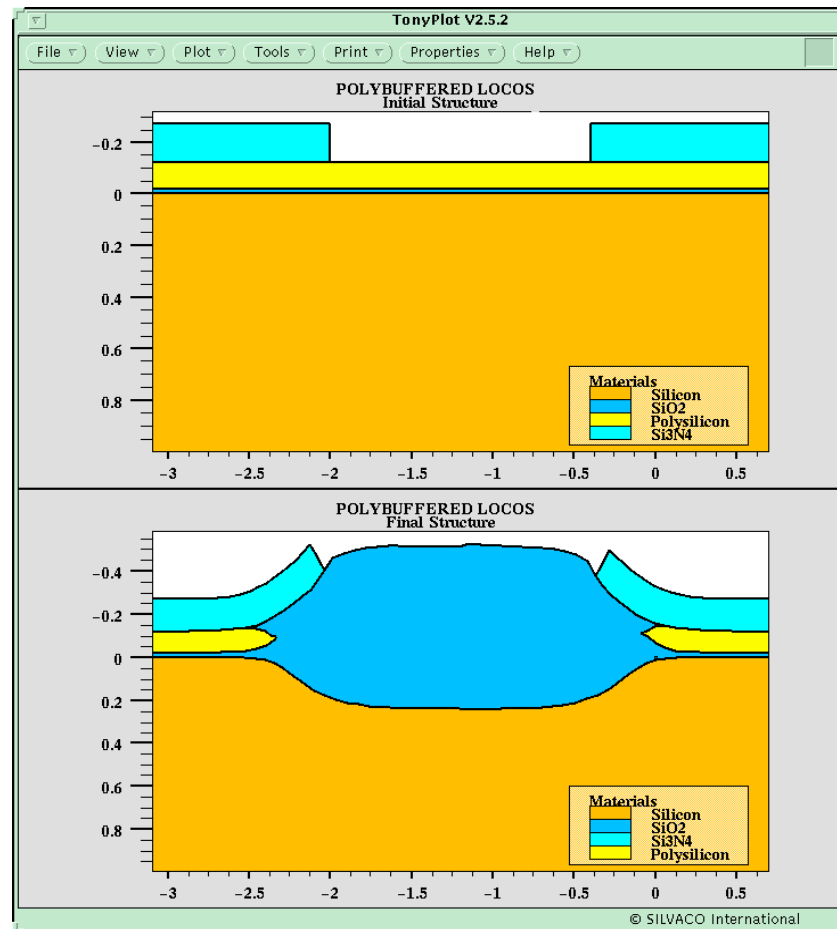


Semirecessed ad Fully Recessed LOCOS



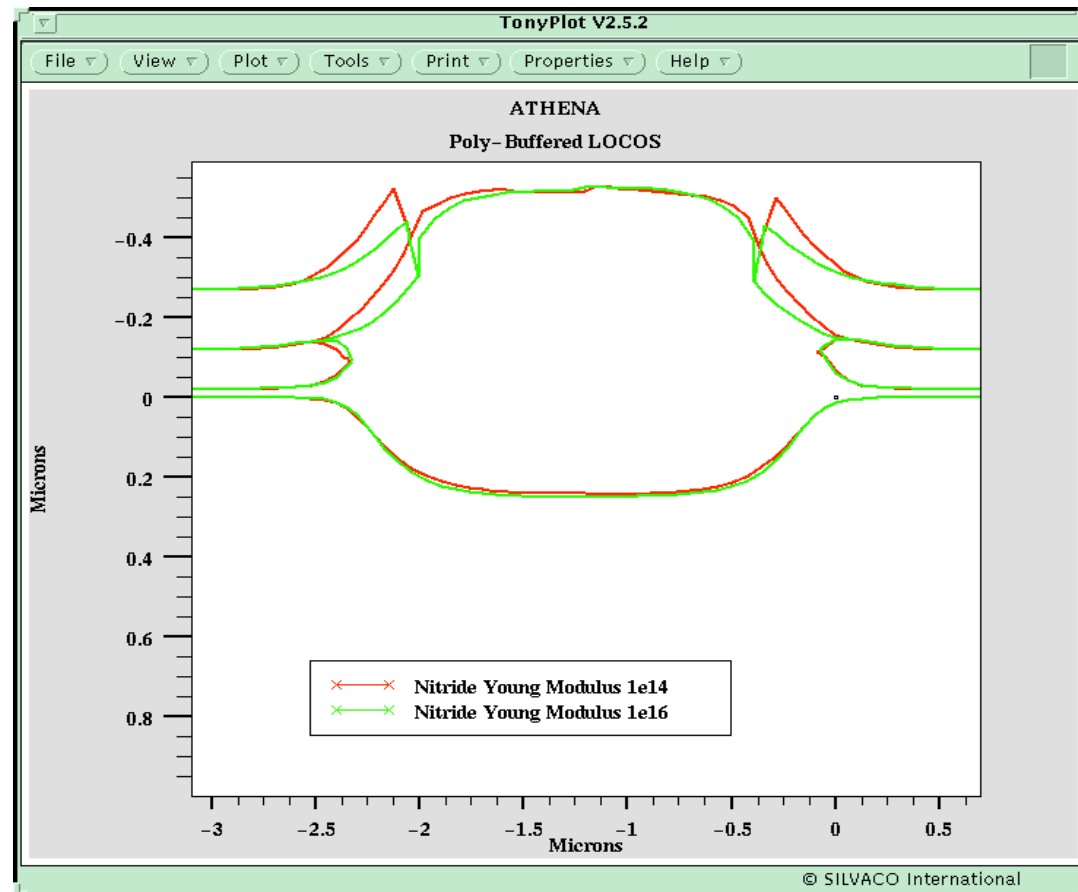


Polybuffered LOCOS Initial and Final Structure



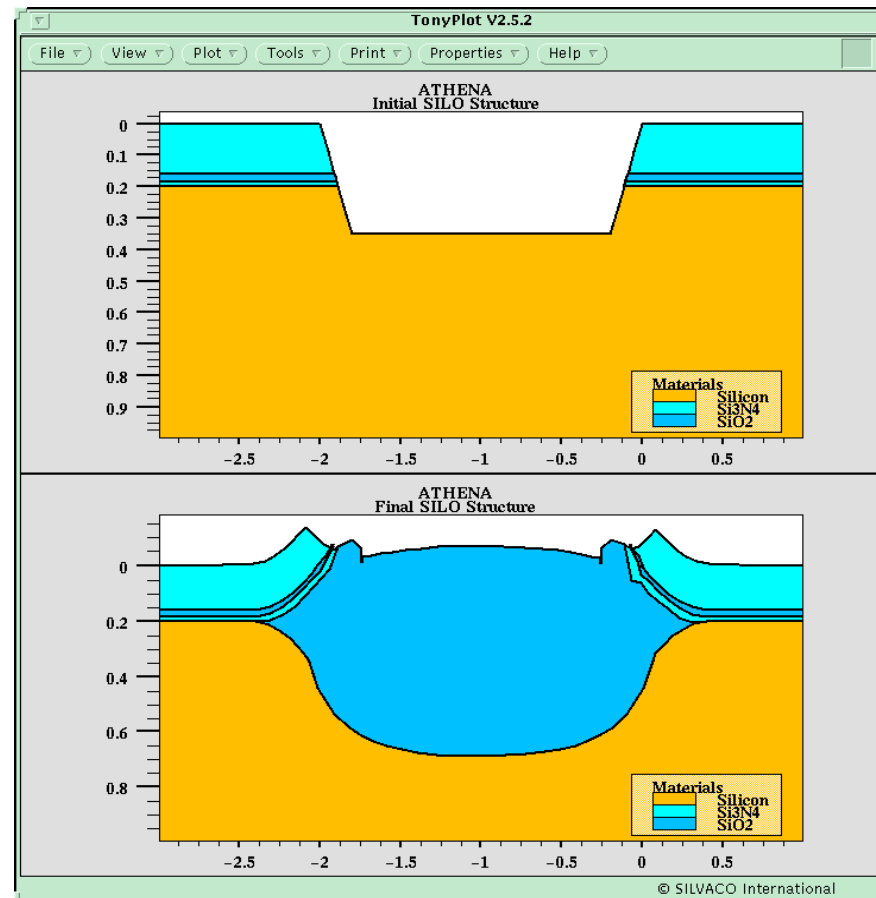


Poly-Buffered LOCOS



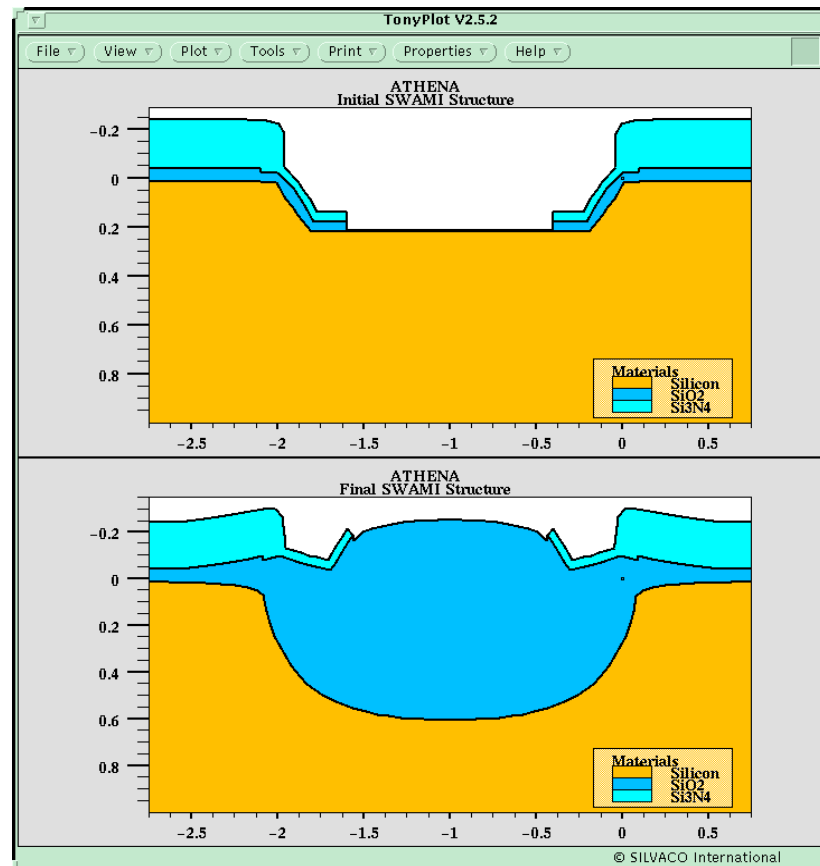


Initial and Final SILO Structure



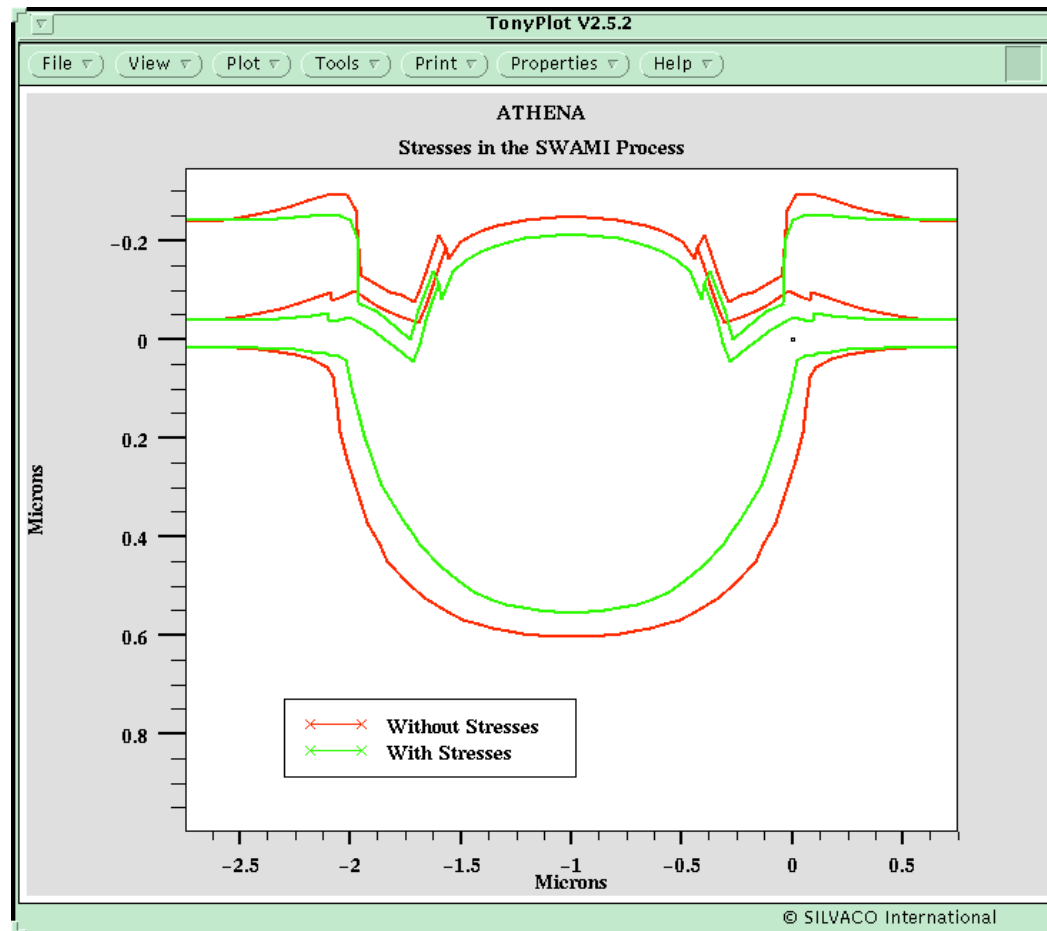


Initial and Final SWAMI Structure





Stresses in the SWAMI Process





Calibration of LOCOS Effects Using VWF

- Several effects typical in LOCOS cannot be simulated without taking stress into account
 - decreasing of bird's beak length (BBL) with increasing of nitride thickness
 - thinning of isolation oxide with narrowing of mask window
 - pad-oxide punch through for narrow patterned nitride
- Global calibration of the model parameters using VWF is needed to predict these effects for different combination of process parameters (e.g.. temperature, nitride thickness and width, pad oxide thickness)

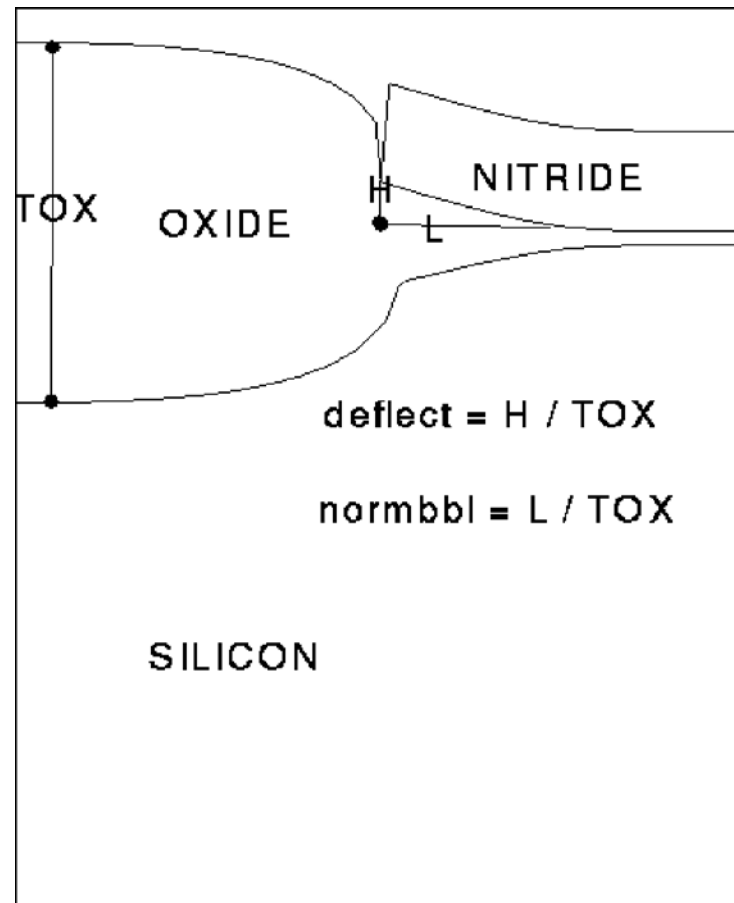


Calibration of LOCOS Effects Using VWF (con't)

- Some calibration results were published in “Simulation Standard”, Aug., 1995
- Figure 7 shows target parameters which can be used in calibration
- Calibration parameters include
 - mechanical properties of oxide and nitride: viscosity, Young modulus, etc.
 - empirical parameters of stress-dependent model:
 - V_d - activation volumes for oxidant diffusivity
 - V_c - activation volume for viscosity
 - V_r - activation volume for oxidation rate



Geometrical Parameters of Birds Beak





Calibration of LOCOS Effects Using VWF (con't)

- It was found by independent experiments that temperature dependence of oxide and nitride viscosity could be presented as follows

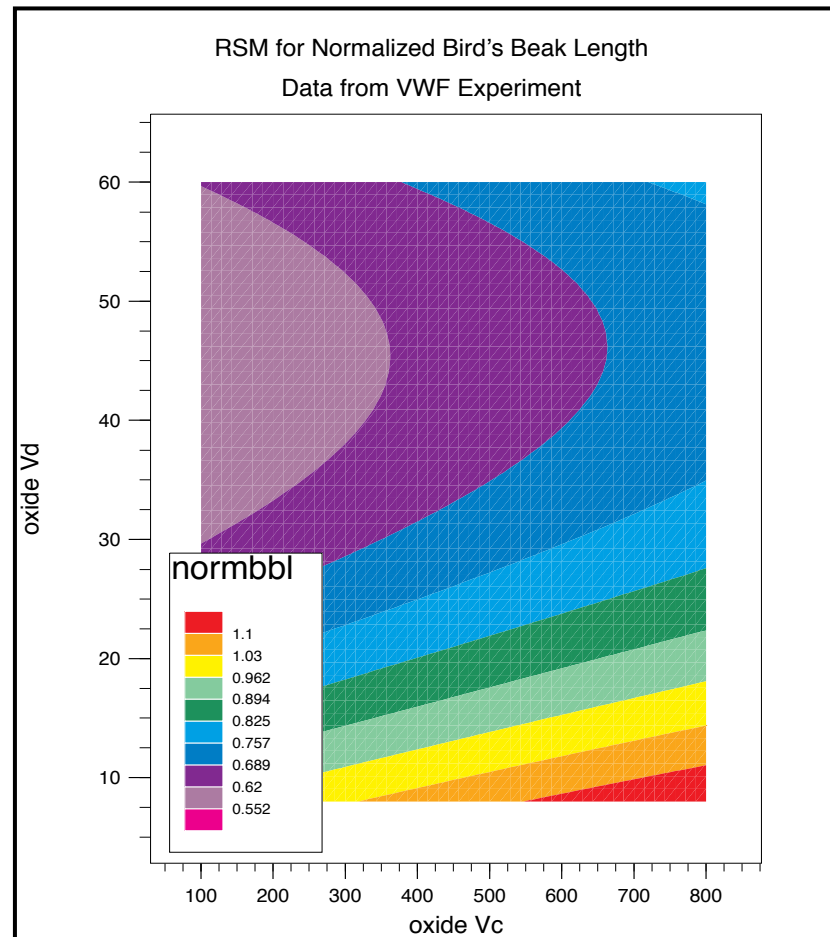
```
material oxide visc.0=5.1 visc.E=3.48
```

```
material nitride visc.0=5.96e5 visc.E=2.5625
```

- Response Surface Models for normalized nitride deflection and normalized BBL were build using a structural Design of Experiment
- Split parameters were oxidation temperature T , nitride thickness T_{nit} , as well as model parameters V_d , V_c , and V_r
- One of the Response Surface Model (RSM) sections is shown in Figure 8



RSM for Normalized Bird's beak Length



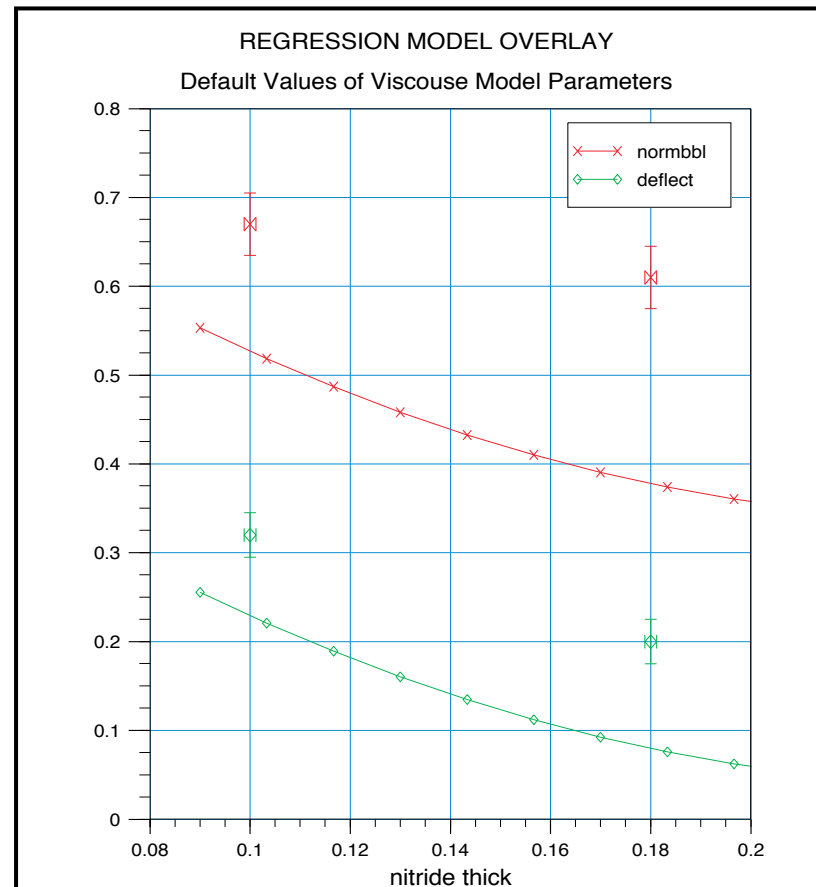


Calibration of LOCOS Effects Using VWF (con't)

- The following shows how BBL and nitride deflection depend on nitride thickness
- It is seen that the RSM simulation results obtained with default model parameters do not match experimental points
- VWF Production Tools allow to manual variations of the input parameters of the RSM with instant graphics of the output.
- Figure 10 shows that even using manual calibration much better agreement with experimental points could be achieved

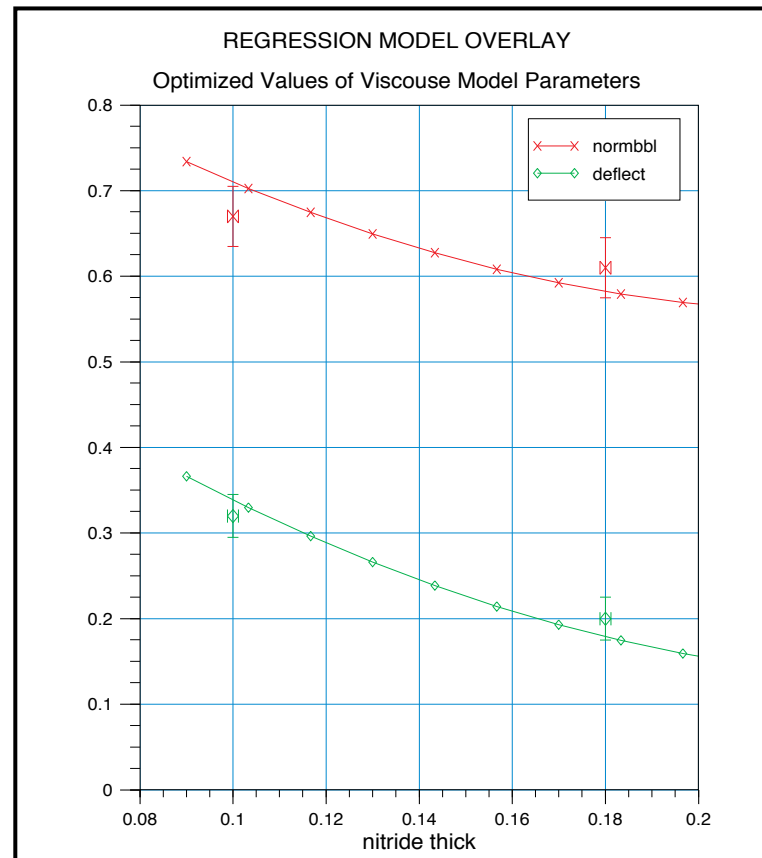


Regression Model Overlay





Regression Model Overlay



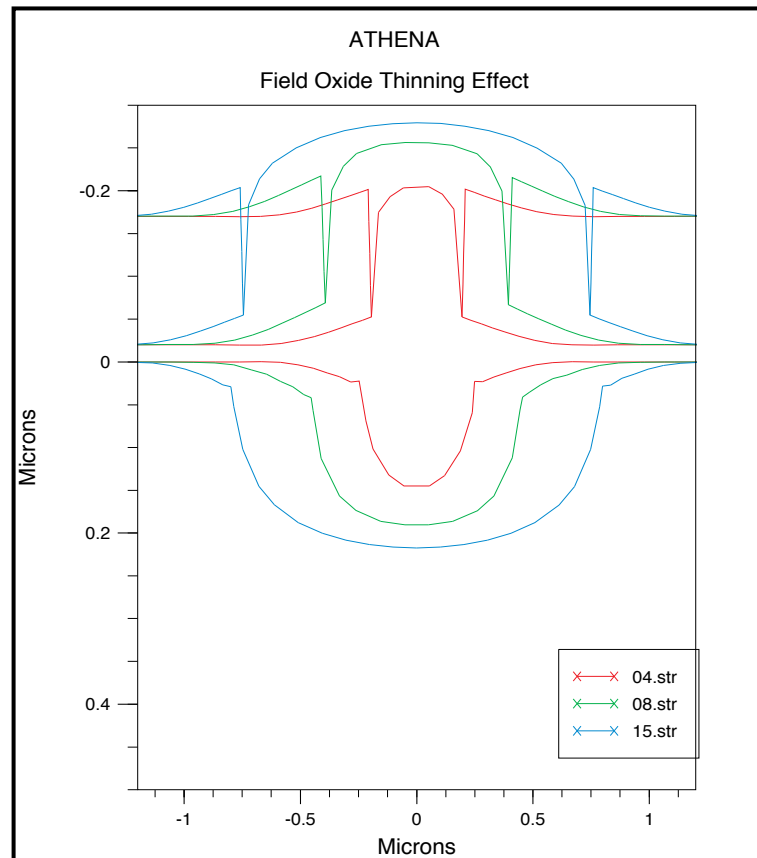


Field Oxide Thinning Effect

- Higher chip density of modern ULSI technology demands shrinkage of isolation areas
- The field oxide thinning effect shown in the figure on page 23 brings about increasing concern to technology designers
- It is seen that the narrower nitride window the more stress-induced retardation of the oxidation rate occurs in the center of the field area
- The figure on page 24 shows that simulation accurately predicts this effect

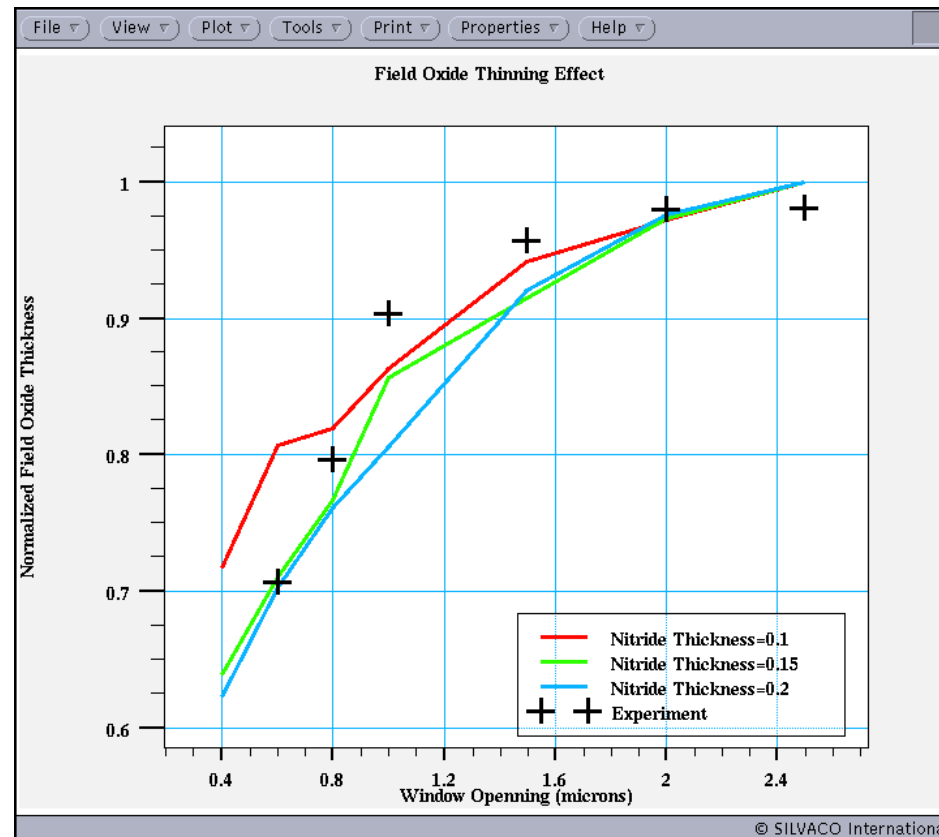


Field Oxide Thinning Effect





Field Oxide Thinning Effect



Field oxide thinning effect for different nitride thicknesses. Experiment for nitride thickness 0.1 micron (P.Coulman et.al., Proc. of 2nd Int. Symp. on VLSI Sci. & Tech., p.759, 1989.)

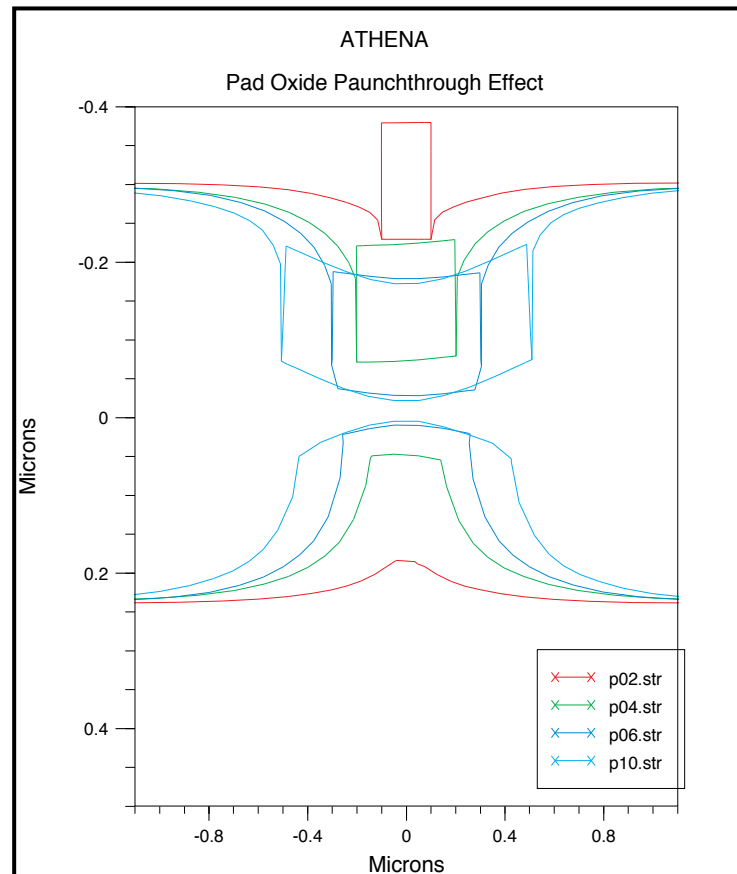


Pad Oxide Punchthrough Effect

- It was found experimentally that bird's beak deflection is quite sensitive to patterned nitride width
- It has a minimum when nitride width decreased to ~ 0.6 microns and then suddenly increases when nitride width decreases further (Figures on page 26 and 27)
- This effect could be explained as follows
 - The highest stresses are built where the highest angle (or curvature) of deflection occurs
 - These stresses retard the local oxidation process
 - When oxidation continues the position of maximum stresses moves toward center of the nitride
 - In case of a narrow nitride the stresses are overcome by oxidant diffusion at some moment after which stresses diminish rapidly and oxide is growing without any obstacles

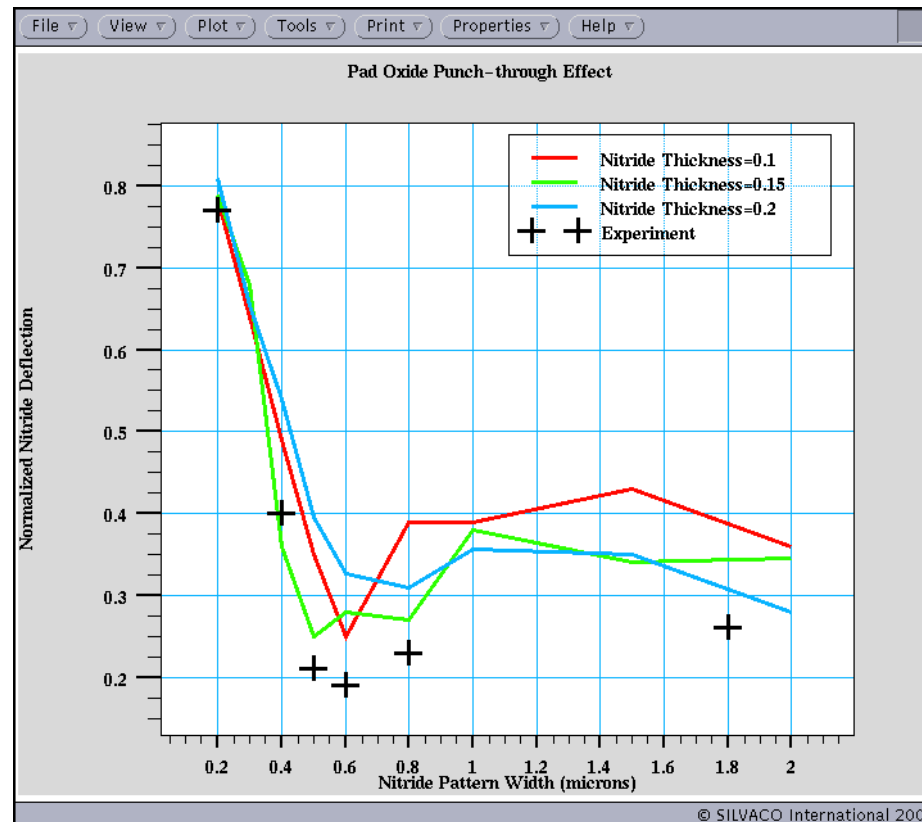


Pad Oxide Punchthrough Effect





Pad Oxide Punch-Through Effect



Normalized nitride deflection versus patterned nitride width for different nitride thicknesses (1000 C, 90 minutes, pad oxide 0.015 micron). Experiment: P.U. Kendale et.al., IEDM Tech. Digest, p.479, 1993.

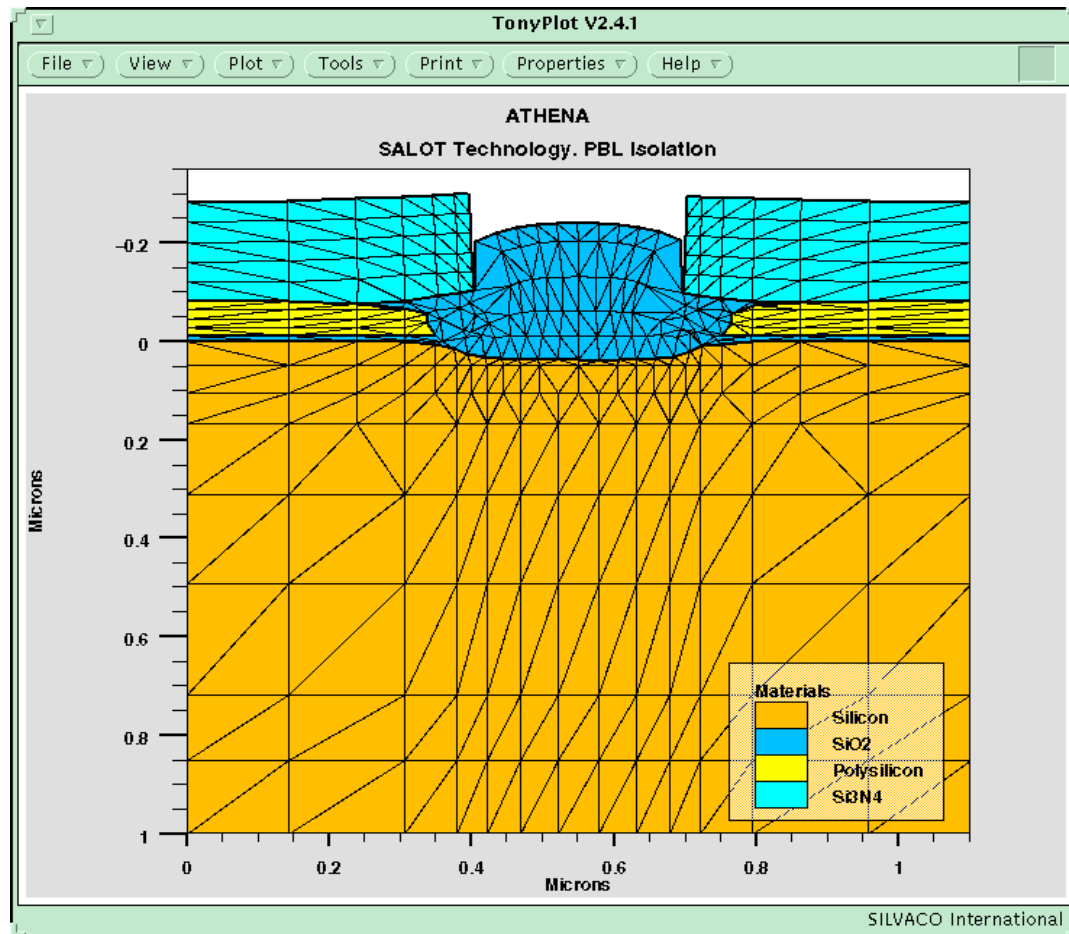


Integrated Topography and In-Wafer Simulation of Self-Aligned LOCOS Trench (SALOT) Technology

- STEP 1. The initial stack of pad oxide (11nm)/ polysilicon(70 nm) / Silicon nitride (200 nm) is defined the same way as for conventional PBL process
- STEP 2. The width of the narrow field region is only 0.3 microns, therefore stress-dependent viscous oxidation model is used here to predict the Field Oxide Thinning Effect for this structure. The mesh used and result of the oxidation are shown in the figure on the following page



SALOT Technology: PBL Isolation



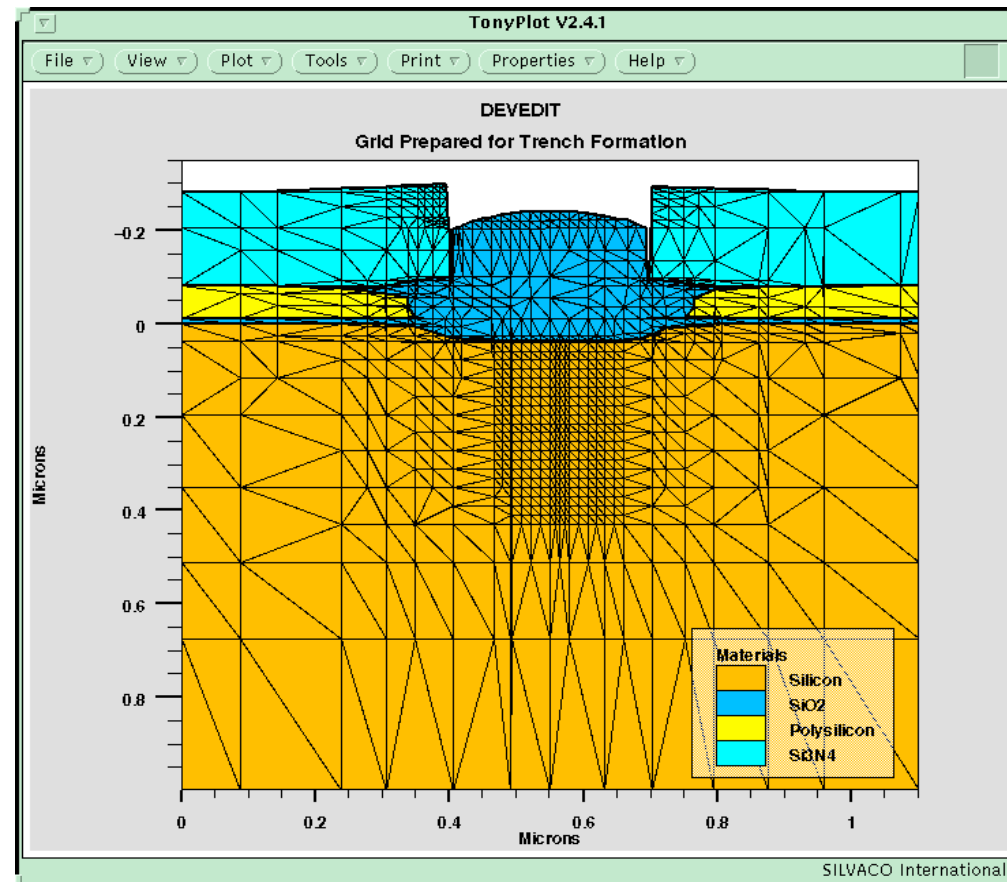


Integrated Topography and In-Wafer Simulation of SALOT Technology (con't)

- To accurately simulate subsequent trench formation steps structure was completely re-meshed using DevEdit (Figure page 31)
- STEP 3. Polysilicon spacers were formed using CVD deposition with subsequent anisotropic etching.
- STEP 4. To achieve self-aligned trench only in the narrow region other areas were masked off (Figure page 32)

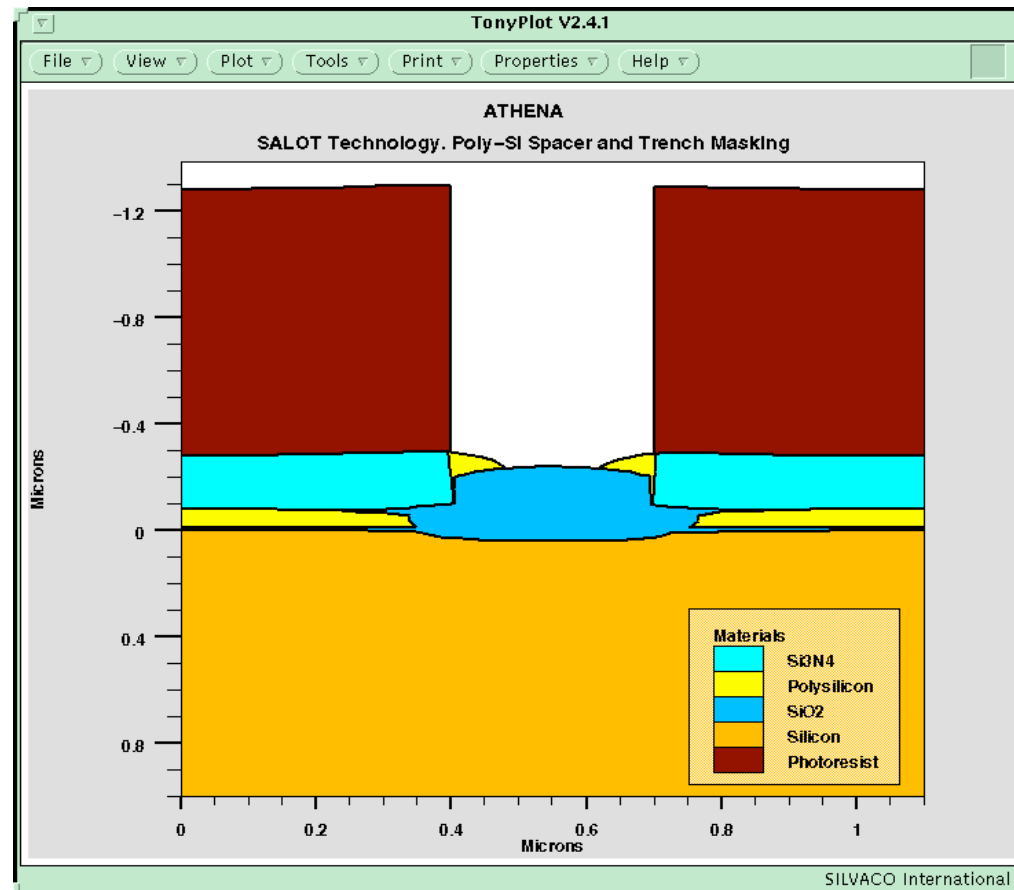


SALOT Technology: Trench Grid Formation





SALOT Technology: Poly-Si Spacer and Trench Masking



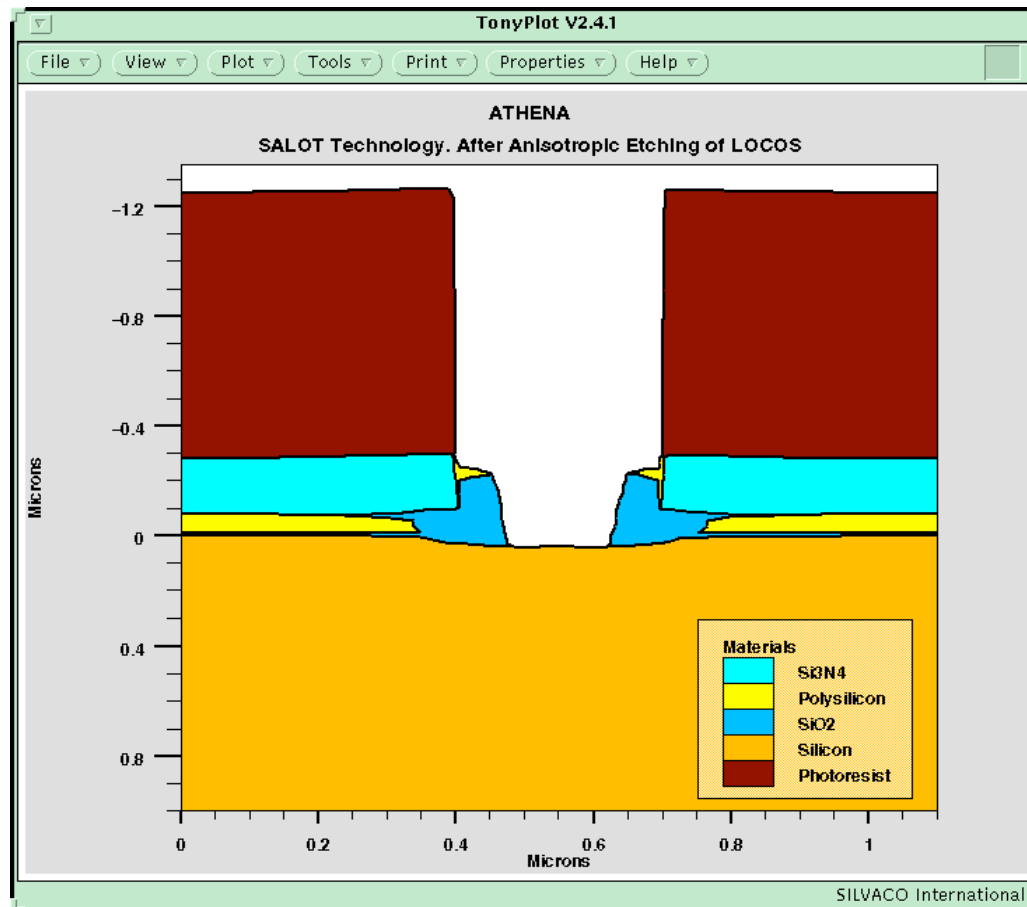


Integrated Topography and In-Wafer Simulation of SALOT Technology (con't)

- STEP 5: plasma etching of exposed LOCOS (Figure page 34). It was simulated using the plasma etching module of ATHENA
- The module calculates energy-angular distribution of ions emerging from plasma using a Monte Carlo calculation. The etch rate in each point is proportional to the ion flux with shadowing and mask erosion taken into account
- The width and shape of etch opening depend on plasma characteristics (temperature, density, etc) as well as on position and shape of the spacers



SALOT Technology: After Anisotropic Etching of LOCOS



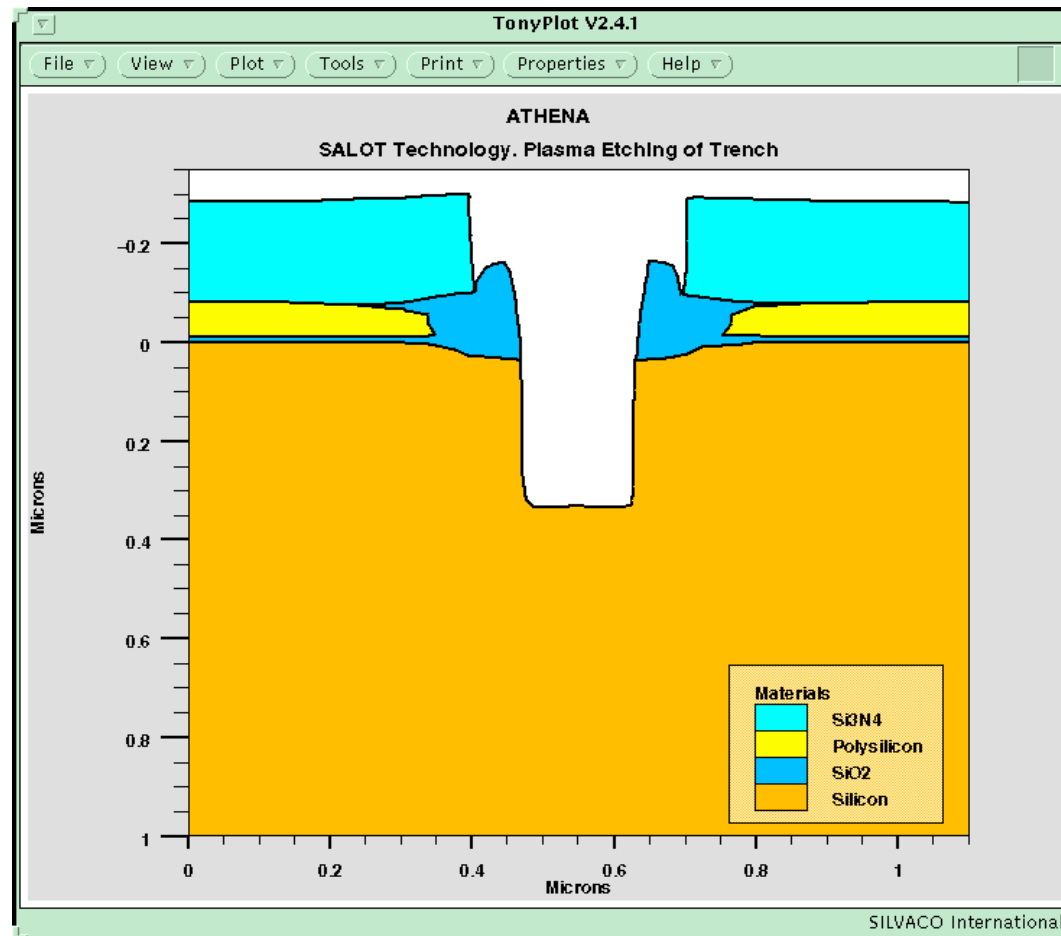


Integrated Topography and In-Wafer Simulation of SALOT Technology (con't)

- STEP 6 is photo mask removal and plasma etching of the 300 nm trench in silicon (Figure page 36)
- In order to illustrate advanced capabilities of ATHENA a sidewall implant step has be added (Figure page 37)

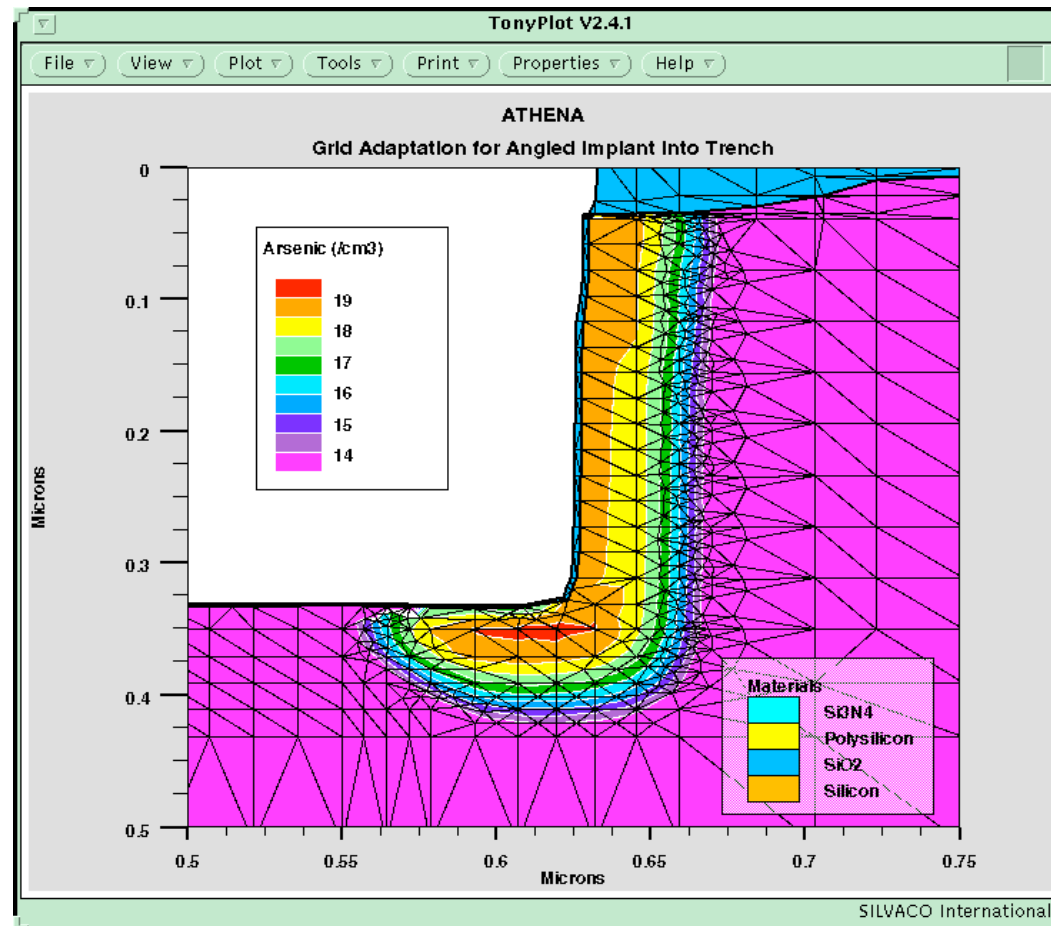


SALOT Technology: Plasma Etching of Trench





SALOT Technology: Side Wall Implantation



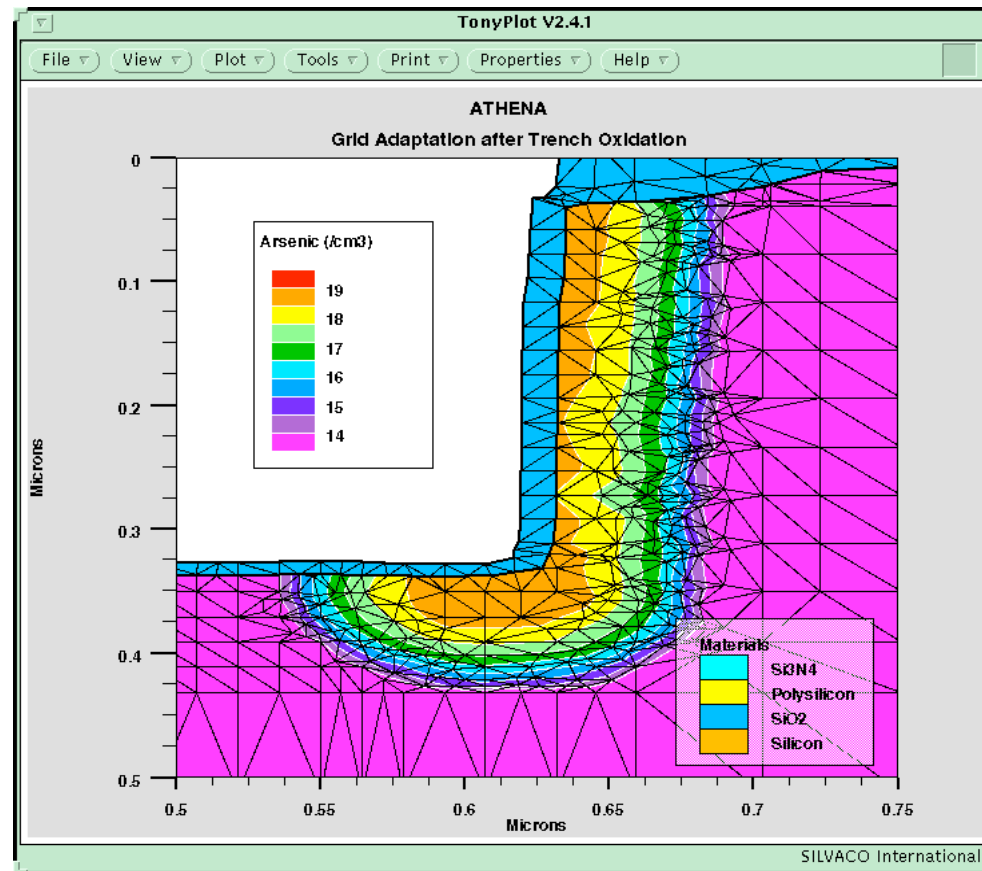


Integrated Topography and In-Wafer Simulation of SALOT Technology (con't)

- STEP 7 is thermal oxidation of the trench with moderate diffusion of just implanted impurity (Figure page 39)
- STEP 8. The trench is filled with oxide. Simple conformal deposition was used in the simulation (Figure page 40)
- STEP 9 is planarization of the field oxide SALOT process using Chemical Mechanical Polishing (CMP). Silicon nitride is served as a masking layer
- This step was simulated using CMP module of ATHENA with polishing rate of nitride 3 times smaller than that of oxide. (Figure page 41)

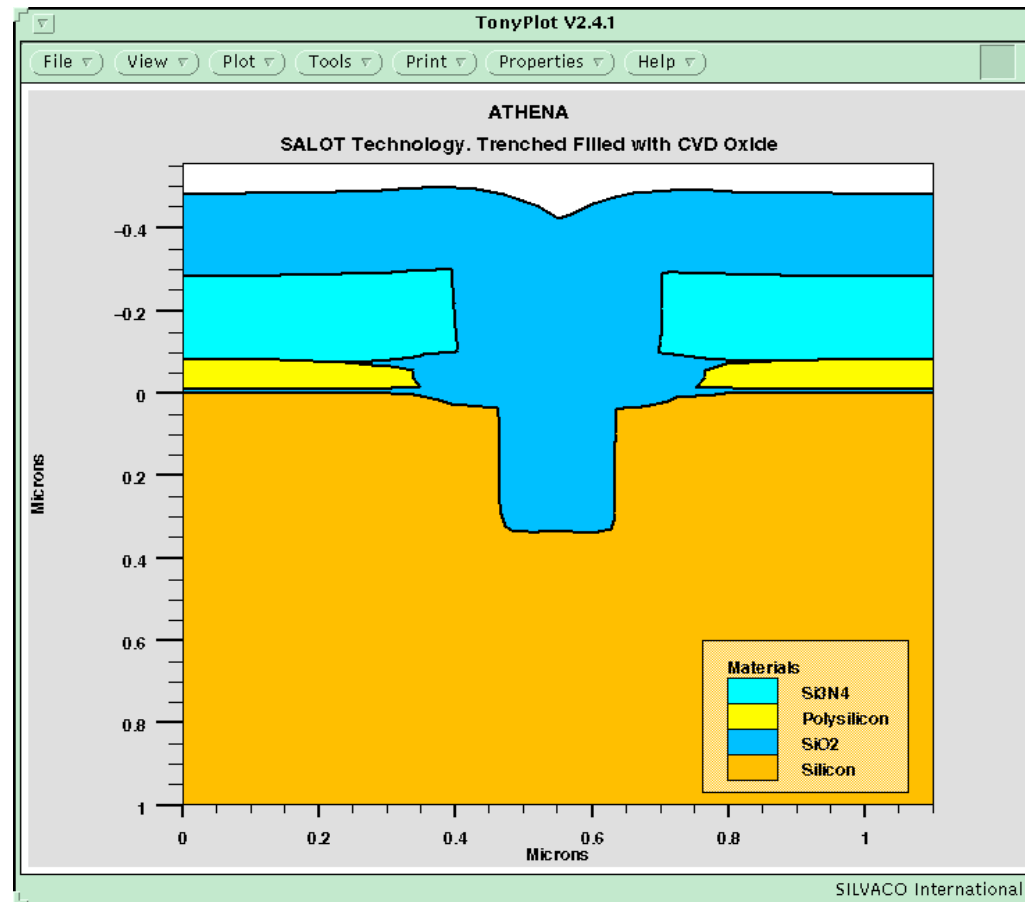


SALOT Technology: Trench Oxidation



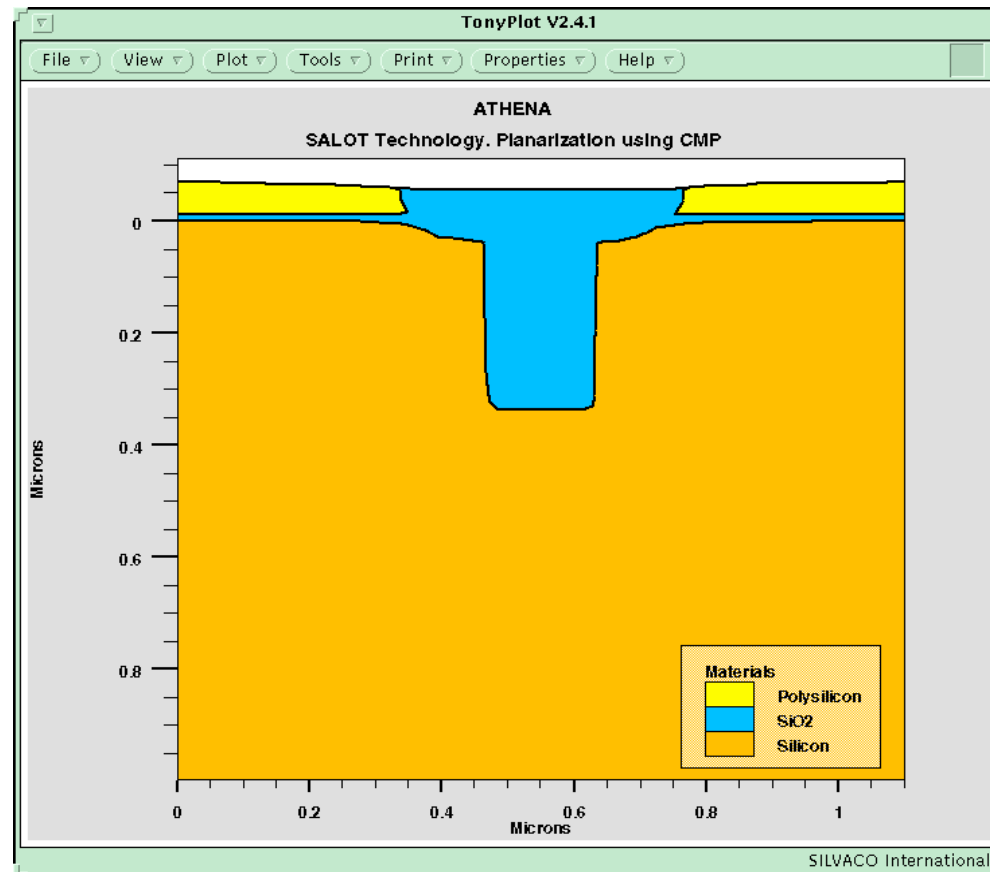


SALOT Technology: Trenched Filled with CVD Oxide





SALOT Technology: Planarization Using CMP





Conclusion

- ATHENA could be successfully used for simulation of different LOCOS geometries
- Stress-dependent model should be used to predict some small CD effects
- The model should be extensively calibrated
- It is shown that VWF could be successfully used for such calibration