

Gateway

Release Notes

02/09/12

RELEASE NOTES

VERSION 2.12.33

ALTERATIONS AND ENHANCEMENTS

- Extract bits from a bus before expanding the bus
- Support “%” character syntax in wire names

VERSION 2.12.32

ALTERATIONS AND ENHANCEMENTS

- Upgrade to SILVACO GUI library to handle GNOME 2.0 fonts

VERSION 2.12.31

ALTERATIONS AND ENHANCEMENTS

- Schematic drawings can be opened from the symbol browser
- Toggle action to hide generated signal names
- Scientific notation format is usable in the Equation Parser
- Library paths now allow environmental variables
- EDIF parser allows UTF-8 support for filenames
- Subtitle frame field updates on Save As
- Chord alias used when expanding bussed pins
- Generate signal names according to the coordinates of the pin or wire
- Add user-definable net name format
- Inform SILOS the schematic root of the design
- Automatically add defparam statements as needed
- Allow instance dependent values when evaluating template strings

VERSION 2.12.30

ALTERATIONS AND ENHANCEMENTS

- Correct the defparam statements in SPICE/Verilog when expanding arrayed instances and when there are multiple instances using defparam statements in subcircuits
- Comma separated signals in the Verilog netlister are correctly expanded for bus manipulation
- The Verilog netlister now always expands buses
- Add input files from non-SPICE simulators into the Design Export

VERSION 2.12.29

ALTERATIONS AND ENHANCEMENTS

- Correction to area selection when selecting multiple wires
- Gateway no longer plots unsupported analyses for appropriate markers

VERSION 2.12.28

ALTERATIONS AND ENHANCEMENTS

- When merging attributes, if an attribute's value on the schematic instance does not reside in the attributes list in the symbol, do not merge the attribute

VERSION 2.12.27

NEW FEATURES

- EDIF writer no longer requires a license

VERSION 2.12.26

NEW FEATURES

- Allow the design browser to be controlled by external applications (e.g., SILOS)
- Allow navigation of the design browser by name

ALTERATIONS AND ENHANCEMENTS

- Correct the Verilog netlist when expanding buses on a pin

VERSION 2.12.25

ALTERATIONS AND ENHANCEMENTS

- Token identifiers are now correctly evaluated in code blocks
- Correct EDIF importer to fix reading of Viewdraw EDIF files
- Use appropriate symbol when determining definition order
- Verilog assignment is now assigned per net instead of per wire segment

VERSION 2.12.24

ALTERATIONS AND ENHANCEMENTS

- Correction where wire identifiers were not being correctly identified for Verilog netlists
- Missing bits of a bus are now defaulted to the bit 1'bz (High impedance) for Verilog netlists

VERSION 2.12.23

ALTERATIONS AND ENHANCEMENTS

- Correct the expansion of arrays when netlisting for Verilog, and the Verilog netlist style is set to one argument per line

VERSION 2.12.22

ALTERATIONS AND ENHANCEMENTS

- Fix the ripping of bits from a bus where the schematic pin attempts to generate a bit incorrectly

VERSION 2.12.21

NEW FEATURES

- Show netlist types (CDL, NDL, Guardian) in the design browser
- Arrayed instances and busses can now be expanded for Verilog netlists using the Expand Busses option

ALTERATIONS AND ENHANCEMENTS

- Resolve wire type when wires are canonicalized
- Correct duplicate instance name check if neither instance name is arrayed

VERSION 2.12.20

NEW FEATURES

- UTF-8 support for filenames
- Each wire type has its own distinct icon in the design browser to easily distinguish the type (e.g., reg, electrical)
- .verilog paths are now supported and paths are resolved in symbol definitions
- New drawing check for nets with different wire types residing on same net

ALTERATIONS AND ENHANCEMENTS

- Fix for resolution of relative paths when exporting a design
- Fix applied for copying/pasting of wire types
- Fix symbol definition reverting to "no definition"

VERSION 2.12.19

ALTERATIONS AND ENHANCEMENTS

- Fix applied for the slowdown of streaming data to the Output tab when SmartSpice writes large amounts of data on Linux

VERSION 2.12.18

NEW FEATURES

- Allow specification of origin point for sheet frames
- Legend position can now be changed in the Frame Settings dialog
- The Wire Attributes dialog now has the ability to specify whether the name change will apply for the local net only or will change the entire supernet. It accomplishes this with the Rename pulldown menu on the dialog.

ALTERATIONS AND ENHANCEMENTS

- Sheet frame sizes adjusted to match ANSI sheet sizes
- Fix for pin rotation on EDIF import
- Fix on the IIF function in the equation parser
- Native OS dialog for Save As action is fixed
- Fix issue of net name visibility when pasting from the Array Paste dialog

VERSION 2.12.17

ALTERATIONS AND ENHANCEMENTS

- Correct missing pins when generating symbols
- Fix an issue with the .global statement due to matching of .global_ in SmartSpice conditions
- Fix a bus expansion issue when expanding prefix multipliers
- Transfer plot data generated from SmartSpice runs when the option to save all the data has been set

VERSION 2.12.16

NEW FEATURES

- CDL control file added for generating specific statements that can be merged into CDL netlists
- View Info Mode has an option to show info bubbles on separate branches of implicit and global nets, including retaining the highlighting color across the nets
- Support for recursive wire tokens (e.g., if %STANDARD_PBULK_NODE is used as an implicit signal name and %STANDARD_PBULK_NODE is set to VDD in the preferences, the netlist resolves them to VDD)
- Frame legends now can be zoomed to view the entire legend and text using Tools → Frame menu

ALTERATIONS AND ENHANCEMENTS

- Fix rotating pins issue during EDIF import
- Prevent crash when checking for dangling wires on old schematics

VERSION 2.12.15

ALTERATIONS AND ENHANCEMENTS

- Default pin directions for EDIF and reading of the symbol file are now correct

VERSION 2.12.14

NEW FEATURES

- New command line option to specify a preferences file to be loaded upon launch of Gateway
- Ability to remove quotation marks around tokens for different netlist strings
- Added netlist line length option to LVS, NDL, CDL, and SPICE netlist formats
- New AMS disciplines added to the wire types list in Wire editing dialog:
 - electrical
 - voltage
 - current
 - integer
 - real
 - wreal
- Now .verilog files are included into the exported archive for Verilog-A

ALTERATIONS AND ENHANCEMENTS

- File format change for schematics. Any schematics saved after version 2.12.12.R cannot be opened by earlier versions of 2.12
- Pin direction warning is turned off by default

VERSION 2.12.13

NEW FEATURES

- Add the netlist order of wires to EDIF files
- Rename all signals if the implicit flag is set

ALTERATIONS AND ENHANCEMENTS

- Case issues for identifiers and ports in EDIF file

VERSION 2.12.12

NEW FEATURES

- Allow wires to be sorted in the Verilog netlister to allow declarations to be used

VERSION 2.12.11

NEW FEATURES

- Supports Cadence CDL netlist generation from Gateway schematics
- Retain Mentor Graphics grid snap spacing for EDIF 200 importing
- When importing SPICE or Verilog libraries containing more than 1000 cells per library, the library is partitioned in groups of 1000 cells for quick searching/instantiation
- New functions in equation parser:
 - ROUND - rounds results to nearest n decimal places
 - CEIL - rounds to next highest integer
 - FLOOR - rounds to next lowest integer
 - ternary operator “?”

For more information about these functions, refer to Appendix E in the Gateway user's manual

ALTERATIONS AND ENHANCEMENTS

- Gateway200 version allows upto a maximum of five X elements or YVLG elements
- Drawing Checks now continue to check for more violations instead of terminating at first encountered error
- “spicelib” library now contains symbols with CDL netlist strings. For new customers, use the “spicelib” that is packaged with the Gateway 2.12.11.R examples. For existing customers who want CDL netlist functionality, you can copy “spicelib” symbols from the 2.12.11.R package into your existing library to replace older symbols.
- Symbols with hundreds of attributes now instantiate quicker by reducing the need for dependency calculations
- For symbol instances, attribute editing is now checked for all attributes (including those not visible in the instance) for boundary conditions