

HyperFault

Release Notes

02/24/12

RELEASE NOTES

VERSION 4.10.132

ALTERATIONS AND ENHANCEMENTS

- Exported code coverage operator report matches GUI report

VERSION 4.10.131

New Features

- New command, “ccmerge”, allows code coverage data files to be merged prior to generating a code coverage report
- “Schematic Root” option in Explorer module tree context menu improves Gateway integration
- User defined file name filters for file open dialogs in program preferences
- New “Open File” option in source editor context menu

ALTERATIONS AND ENHANCEMENTS

- Project file key fields accept numbers with leading zeros

VERSION 4.10.130

ALTERATIONS AND ENHANCEMENTS

- Signedness of memory elements is now set correctly
- Improve code coverage “Operator” report generation speed
- Missing include files generate warnings, not errors, during library scanning

VERSION 4.10.129

ALTERATIONS AND ENHANCEMENTS

- Terminal names for some Verilog primitive devices (e.g. notif0, notif1, nmos, pmos) returned by `acc_fetch_name()` now match the IEEE-1364 standard
- Log file for GUI version of program enabled by default
- Improve code coverage “Operator” and “Branch” reports for multiple module instances
- Improve “Warning” command

VERSION 4.10.128

ALTERATIONS AND ENHANCEMENTS

- Excluding faults with "PLI" type names now works as intended

VERSION 4.10.127

ALTERATIONS AND ENHANCEMENTS

- SILOS extension options reset when program is reset
- Code Coverage report merge option accepts duplicate entries in the merge file

VERSION 4.10.126

NEW FEATURES

- Add " Merge" option for Activity reports
- Add new system task, \$dumpactivity() to support Activity report " Merge" option

Alterations and Enhancements

- \$record_fault_data() system task now works as documented in the User's Manual
- VCD \$version section now includes \$dumpfile task
- Harmony specific items removed from Edit menu

VERSION 4.10.124

ALTERATIONS AND ENHANCEMENTS

- Negative integers can cause an infinite loop in Lint code

VERSION 4.10.123

NEW FEATURES

- Modify toggle report to show single transitions as H->L or L->H

VERSION 4.10.121

NEW FEATURES

- Add a Scope edit box to Explorer that displays the full hierarchical path of the selected module in the tree view
- Add a communication link that will send " Scope" messages to Gateway. This will allow the Gateway Design Browser tree to be updated when a module is selected in the Explorer tree. This feature will work with Gateway version 2.12.26 and higher.
- Explorer file tree display, add action, double click on file name will open file in editor window

ALTERATIONS AND ENHANCEMENTS

- Analyzer sometimes does not draw all signal states

VERSION 4.10.120

ALTERATIONS AND ENHANCEMENTS

- Output variable initialization in a port declaration statement causes errors. The program now supports this syntax: "output reg myreg = 1'b1;"
- rtranif0, rtranif1 primitive instance with hierarchical connection causes program exception during source file parsing

VERSION 4.10.119

ALTERATIONS AND ENHANCEMENTS

- " end" and " endgenerate" on a single line causes errors in a generate block
- " end" and " else" on a single line causes errors in a conditional generate block

VERSION 4.10.118

ALTERATIONS AND ENHANCEMENTS

- Code Coverage branch report missing some " if" statements

VERSION 4.10.115

ALTERATIONS AND ENHANCEMENTS

- Simulation speed slower than expected (Windows only)

VERSION 4.10.114

ALTERATIONS AND ENHANCEMENTS

- Cannot save project if null project file exists
- File->Save As menu item disabled if file is opened using error message hypertext link
- File dialogs have Windows resource leaks
- Different results between Analyzer and SmartView for vectors with reversed msb/lb order

VERSION 4.10.113

ALTERATIONS AND ENHANCEMENTS

- Library file paths that include Unicode characters were written to .cfv file with ucs2 encoding should be utf8
- Certain test cases cause program errors during simulation if SmartView is the selected viewer
- The program error when reading project files that contain null value strings
- Support for Unicode/UTF-8 file paths missing for Lint
- Output window does not display Unicode file paths correctly

VERSION 4.10.112

NEW FEATURES

- Add +ghdl_format command line option This command line option works with the \$vcdin() system task. The GHDL simulator may include 'U' value characters in the 4 state VCD files it can generate, this is not a legal 4 state value character as specified in the IEEE 1364 LRM. The +ghdl_format option will translate the illegal 'U' value characters to 'X' value characters.
- Add support for Unicode/UTF-8 file paths

ALTERATIONS AND ENHANCEMENTS

- Extended VCD output format incorrect
- Analyzer display group signals are not saved/restored in the same order
- File->Save Project menu item does not update Analyzer signal groups
- Using the menu item Debug->Restart simulation causes an error message on Linux: "MainWinBase::restartSimulationSlot(): Not implemented yet."

VERSION 4.10.111

NEW FEATURES

- Allows the user to specify save file name in Simulation Data File dialog

VERSION 4.10.110

ALTERATIONS AND ENHANCEMENTS

- Extended VCD output did not include the \$vcdclose entry if program is run in the command line mode
- Local variable initialization in tasks and functions caused core dump (invalid syntax)
- Incomplete library statement should generate error message
- Using Load/Reload after breaking out of zero delay loop causes a program error

VERSION 4.10.108

ALTERATIONS AND ENHANCEMENTS

- Certain parameter definitions that contain forward references cause program errors or incorrect results

VERSION 4.10.107

NEW FEATURES

- Add " Save Project" selection to File menu

ALTERATIONS AND ENHANCEMENTS

- Function example causes program error (related to invalid function declaration)

VERSION 4.10.106

ALTERATIONS AND ENHANCEMENTS

- Project file corrupted if Windows 7 Sync Center is used
- Program sometimes seg faults while restoring simulation (Linux)

VERSION 4.10.104

NEW FEATURES

- Allow user to select Analyzer font

ALTERATIONS AND ENHANCEMENTS

- QT debug message prints to stdout
- Using Trace Inputs causes acc error messages
- Watch window selection incorrect after new signal has been added
- File->New Project does not clear existing file

VERSION 4.10.103

NEW FEATURES

- Add an option to display full path in Explorer tree to Edit->Program->Options dialog
- Add an option to allow user to select system or QT generated file dialogs. See Edit->Program->Options dialog. Using the QT dialogs may eliminate some Windows 7 related issues.

ALTERATIONS AND ENHANCEMENTS

- C-Style parameters are not listed in Explorer listview
- Error " Invalid number of processors m, reset to n" should be a warning.

VERSION 4.10.101

ALTERATIONS AND ENHANCEMENTS

- Add a warning for timing checkers: Only one '&&&' operator is allowed by the IEEE 1364 standard
- Valid `ifndef statement causes error message
- Automatic task/function keyword causes error message
- Missing argument from \$width statement causes error message. Although the LRM states that the threshold argument is required if the notifier argument is specified, this syntax is allowed by another Verilog simulator. Changed the error to a warning message.
- Unnamed generate blocks cause syntax errors

VERSION 4.10.100

ALTERATIONS AND ENHANCEMENTS

- Reloading a source file that contains VCD system tasks causes program error

VERSION 4.10.99

ALTERATIONS AND ENHANCEMENTS

- Project file wiped out when new Signal Group is added to analyzer
- Analyzer Signal Groups disappear while simulation is running, not reloaded at \$finish or pause
- Shortcut keys do not work after reload and run

VERSION 4.10.98

NEW FEATURES

- Highlight variables in watch window if the value has changed while single stepping

ALTERATIONS AND ENHANCEMENTS

- UDP instance in a generate block causes an error
- Null statements in generate block should be errors
- Parser does not allow full range of floating point values
- Option "save `celldefine data" should default to "on"
- Project file wiped out when new Signal Group is added to analyzer
- Analyzer Signal Groups disappear while simulation is running, not reloaded at \$finish or pause

VERSION 4.10.96

ALTERATIONS AND ENHANCEMENTS

- Program Properties directory browser not working as intended
- Removed Debug->Break menu item
- \$fwrite system task adds an extra newline to the output file if opened as a multi-channel descriptor

VERSION 4.10.95

ALTERATIONS AND ENHANCEMENTS

- Program not working as intended with sencrypted files
- Selecting Verilog primitives in Explorer or Analyzer cause error message or program error

VERSION 4.10.94

NEW FEATURES

- Add a command line option to flush simulation data file periodically

VERSION 4.10.93

ALTERATIONS AND ENHANCEMENTS

- Invalid simulation data file path written to .cfv file
- PLI routines cause errors or program exception

VERSION 4.10.92

NEW FEATURES

- Analyzer: Add marker and Tdelta time values to waveform window. This feature is enabled in the Edit->Preferences->Waveform Viewer->Analyzer Options dialog
- Analyzer: Enable left arrow and right arrow keys for scrolling waveform window

VERSION 4.10.91

ALTERATIONS AND ENHANCEMENTS

- Strange behavior when text macro is redefined in a library file