

# Spider

Release Notes

3/13/12

## RELEASE NOTES

### VERSION 1.6.1

#### NEW FEATURES

- Baseline Release

### VERSION 1.4.3

#### ALTERATIONS AND ENHANCEMENTS

- LOAD\_DESIGN GDSII to LEF eliminate duplicate data in source file from output
- LOAD\_DESIGN .lyr file obstruction object processing concurrent with pin data when overlaps exist
- LOAD\_DESIGN <design\_name>.net.statistics reports the top fanout nets and vital statistics

### VERSION 1.4.2

#### NEW FEATURES

- DSPFGEN RC parasitic extractor in DSPF format for both pre-placement and post-route
- CATALYSTLL Liberty pre-processor utility with bus syntax support and format unification

### VERSION 1.4.1

#### NEW FEATURES

- TIMEGEN timing constraint translator from SDF to TIM format
- CATALYSTDD utility for flattening and bus expansion of Verilog netlists

### VERSION 1.4.0

#### NEW FEATURES

- Native 64-bit Red Hat Enterprise 4 release

## **VERSION 1.3.9**

### ALTERATIONS AND ENHANCEMENTS

- Reverse OPIN, IPIN, CKPIN direction in generated Verilog from VERILOGGEN

## **VERSION 1.3.8**

### NEW FEATURES

- "vert\_block\_pin\_layer" and "horiz\_block\_pin\_layer" options in .load file for LOAD\_DESIGN to expand user control over layer definition
- "cover=" option in .load file for LOAD\_DESIGN. Add cover data to CHIP\_PHYSICAL\_TYPE in PDL

### ALTERATIONS AND ENHANCEMENTS

- Output in DDL file the max timing arc data from multiple similar arcs in LOAD\_DESIGN
- OPIN and IPIN take default inverter timing info from LOAD\_DESIGN .load file "clock="option
- Change OPIN and IPIN in PDL file generated by LOAD\_DESIGN from 1x1\_PIN cell to 2x2\_PIN cell
- Change CKPIN in PDL file generated by LOAD\_DESIGN from 2x1\_PIN cell to 3x1\_PIN cell
- Adjust POS statement in CDL file generated by LOAD\_DESIGN for OPIN, IPIN and CKPIN size change and remove co-adjacent PG rail pin site locations to eliminate routing congestion

## **VERSION 1.3.7**

### NEW FEATURES

- "add\_onetarget\_pin\_vias" option in .load file for LOAD\_DESIGN to add OPTVIA in PDL to improve routability
- OPIN, IPIN, CKPIN, BPIN, PPIN and GPIN placement location control by user defined "pif=" file using CDL file POS statement generated by LOAD\_DESIGN

### ALTERATIONS AND ENHANCEMENTS

- Adjust DEF file DIEAREA x-offset generated by V2DEF/LOAD\_DESIGN when non-zero origin exists
- Improve Verilog module top level ports generation from VERILOGGEN

## **VERSION 1.3.6**

### ALTERATIONS AND ENHANCEMENTS

- Extend DEF output file "+NEW" syntax for DEFGEN to also include pre-route NETS data in addition to existing pre-route PIN data

## **VERSION 1.3.5**

### ALTERATIONS AND ENHANCEMENTS

- Change GRDGEN "check\_obst" option default value from false to true
- Change "systemnames" global option default value from false to true in REDIT, PGREDIT, RDUMP, PGRDUMP, RLOAD and PGRLOAD
- Improve Verilog escaped name handling for VERILOGGEN

## **VERSION 1.3.4**

### ALTERATIONS AND ENHANCEMENTS

- Round DDL file values generated by LOAD\_DESIGN when reading Liberty .lib containing values with higher than allowed precision

## **VERSION 1.3.3**

### ALTERATIONS AND ENHANCEMENTS

- Liberty .lib version 2.4 update for LOAD\_DESIGN .load "lib =" command
- Improve rip-up routing completion rate for RROUTE/REDIT

## **VERSION 1.3.2**

### **NEW FEATURES**

- Import GDSII file with "gdsii =" and "lyr =" options in LOAD\_DESIGN .load file and convert to LEF macro file, replaces GDS2LEF

### **ALTERATIONS AND ENHANCEMENTS**

- Significant Verilog import speed up for LOAD\_DESIGN

## **VERSION 1.3.1**

### **NEW FEATURES**

- DEF file SCANCHAINS statement for LOAD\_DESIGN
- Scan chain reordering with SCANCHAIN utility
- GDS2LEF standalone layout conversion from GDSII to LEF macro file utility

### **ALTERATIONS AND ENHANCEMENTS**

- Extend .tdl file LINE\_SPECS statement for LEF technology file PITCH and OFFSET control and/or DEF file TRACKS statement handling for LOAD\_DESIGN

## **VERSION 1.2.9**

### **ALTERATIONS AND ENHANCEMENTS**

- LEF .tech file SPACING RANGE for wide metal processing for LOAD\_DESIGN

## **VERSION 1.2.8**

### **NEW FEATURES**

- BACKANNOTATE performs SDF timing constraint and RC parasitic backannotation, replacing obsolete SL2SDF PERL script method

## ALTERATIONS AND ENHANCEMENTS

- LEF .tech file MANUFACTURINGGRID processing for LOAD\_DESIGN
- Leaf cell layout data grid checking and reporting for LOAD\_DESIGN

## **VERSION 1.2.7**

### ALTERATIONS AND ENHANCEMENTS

- Change MASKOUT external name generation for LVS checking

## **VERSION 1.2.6**

### ALTERATIONS AND ENHANCEMENTS

- Modify DEFGEN to permit execution at ANY point in the design flow after PCOMP compilation
- Permit use of both stacked and unstacked via data structures for DEFGEN
- Modify VERILOGGEN to permit execution at ANY point in the design flow after PCOMP compilation

## **VERSION 1.2.5**

### ALTERATIONS AND ENHANCEMENTS

- Change layout data checking and error polygon removal processing in Contour Router DRC error avoidance engine for PGREDIT