

# SILVACO

## VERILOG SIMULATOR

# SILOS

SILOS is an easy-to-use IEEE-1364-2001 compliant Verilog simulator used by leading IC designers. An industry standard since 1986, its powerful interactive debugging features provide today's most productive design environment for FPGA, PLD, ASIC and custom digital designs.

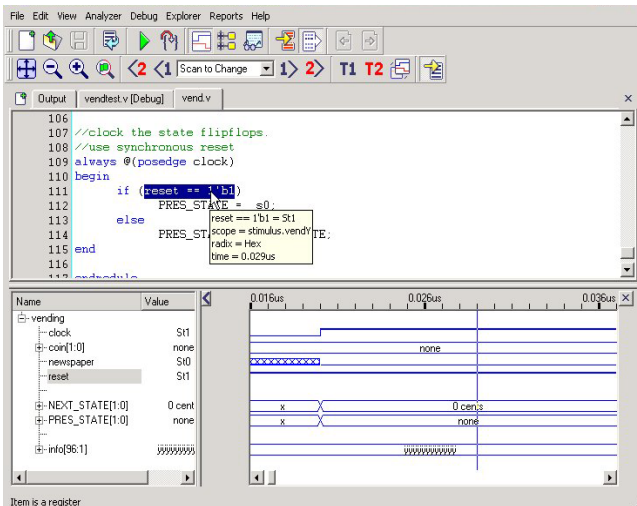


- **IEEE-1364-2001 compliant Verilog simulator with Programming Language Interface (PLI) supports language extensions**
- **Productive debugging environment with graphic data analyzer, trace mode, hierarchy explorer, and interactive source code editor**
- **Embedded lint tool that can make comprehensive syntax, semantic and design rule checking with over 500 checking rules. Can check for simulation and synthesis mismatches, race condition, clock domain synchronization and more**
- **Ensures comprehensive verification with integrated code coverage**
- **Supports compliance testing for RTCA/DO-254, "Design Assurance Guidance for Airborne Electronic Hardware," Appendix B**
- **Silvaco's strong encryption is available to protect valuable customer and third party intellectual property**

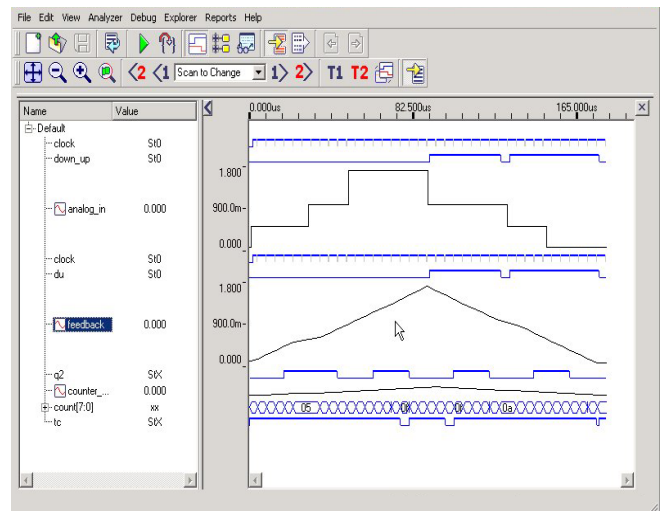


## Productivity – Interactive Simulation Environment

- High Performance simulation engine achieves fast simulation results rivaling compiled Verilog for interactive debugging of designs up to several hundred thousand gates—with no compile times
- Interactive, interpreted Verilog environment provides a set of multi-tasking utilities to edit HDL source, set incremental breakpoints, stepping or timed simulation, real-time viewing, and error detection
- Multi-window customizable Data Analyzer controls pan and zoom, timing markers, using interactive “drag & drop” capture, and display for signals and expressions for analog and digital waveforms
- Trace Mode graphically traces all fan-in connections to any signal through all levels of circuit hierarchy instantly
- Watch window displays or forces state values of specified signals and variables while single-stepping—all set up through “drag & drop” for designer convenience



Data Tips in the Source Window display value, scope, and time of the highlighted expression at the T1 marker in the Data Analyzer.



Analog waveforms can be displayed in either piecewise linear format or stepping format.

## Lint Capability

- Checks for more than 500 design rules
- Checks race conditions and clock domain synchronization
- Checks for synthesizability, and reports potential synthesis and simulation mismatches
- Optimizes gate usage with detailed reports of inferred registers, latches, state-machines and other sequential elements that will be synthesized into synchronous hardware
- Extracts Finite State Machines (FSM) and analyses for redundant or unreachable states
- Offers design-for-testability checks for up-front identification of un-testable circuits
- Comprehensive report filtering system delivers precise information to isolate and fix problem

## Support for FAA Standard D0254 Testing

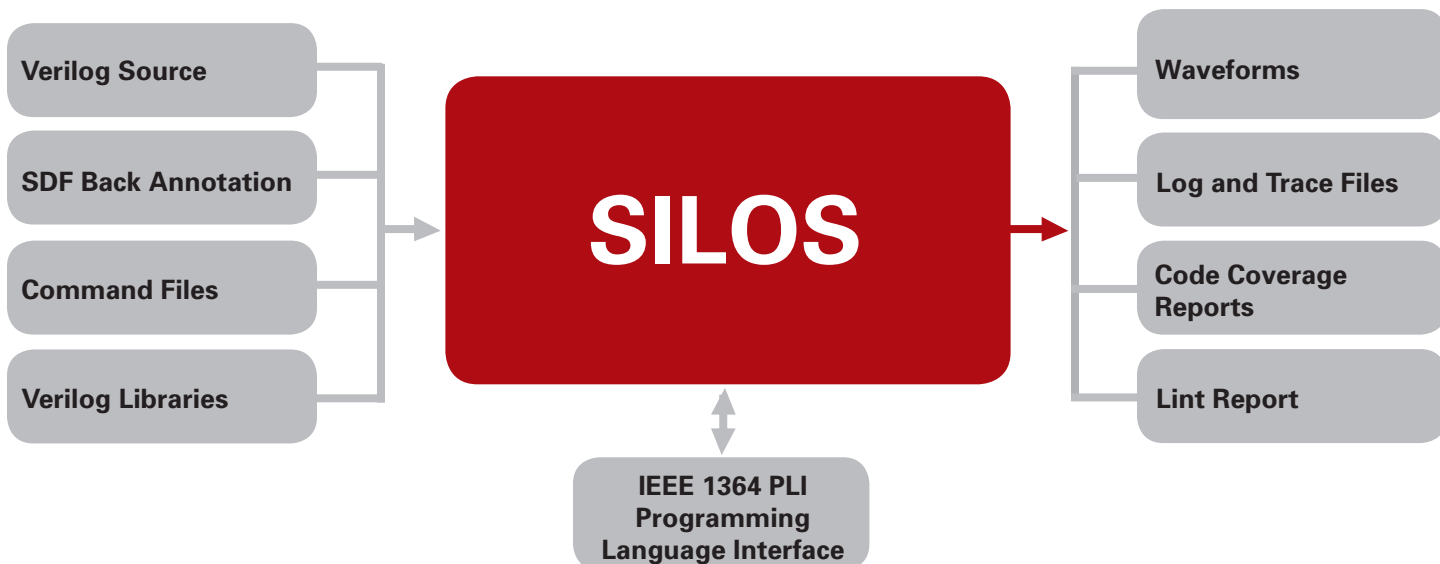
RTCA/DO-254, DESIGN ASSURANCE GUIDANCE FOR AIRBORNE ELECTRONIC HARDWARE is a standard recognized by the Federal Aviation Administration (FAA) as a means to ensure the safety of electronic airborne systems by verifying the design of complex electronic hardware in airborne systems.

The SILOS code coverage reporting feature supports compliance testing for RTCA/DO-254 "Design Assurance Guidance for Airborne Electronic Hardware," for levels A and B as specified to meet "Elemental Analysis" in Appendix B.

SILOS generates code coverage reports including "Line/Statement Coverage," "Operator/Expression Coverage" and "Branch Coverage." Reports can be exported as text files and can also be examined interactively using the SILOS graphical user interface (GUI). Code Coverage data from multiple independent simulation runs can be merged into a single report.

The user can enable and disable coverage reporting for specific lines and blocks of behavioral source code. Spurious time 0 events are automatically eliminated from the coverage results.

## SILOS Inputs/Outputs



# SILVACO

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Rev. 081811\_22